Tandy 200 Technical Reference Manual
26-3861

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CONTENTS

List of Illustrations

List of Tables

INTRODUCTION

Tandy 200 portable computer is an enhanced version of the Radio Shack Model 100 Portable Computer. The Tandy 200 is software compatible with the Model 100 in BASIC so that both system users can take advantage of the large number of programs available.

One important difference between the Model 100 and Tandy 200 is the size of the LCD screen. The Tandy 200's LCD screen is double the size of the Model 100's. That is, the Model 100's display capability is 40 × 8 characters while the Tandy 200 has a display capability of 40 × 16 characters.

The Tandy 200 has the following applications programs in the standard ROMs: BASIC, TEXT, ADDRSS, SCHEDL, TELCOM, MSPLAN, and ALARM.

External View

1 **Keyboard.** Can be used like the standard typewriter. However, the Tandy 200 does have a few special keys. (See Appendix B of this manual for more details.)

2 **LCD Unit.** The Tandy 200 display has sixteen lines that allows 40 characters on each line.

3 **POWER Switch.** Push this switch to turn the power ON or OFF. To conserve the batteries, the Tandy 200 automatically turns the power off if you do not use it for 10 minutes.

4 **Low Battery Indicator.** Before the Tandy 200's operational batteries become exhausted, this indicator will illuminate.

5 **Display Adjustment Dial.** This control adjusts the contrast of the LCD display relative to the viewing angle.

6 **External Power Adapter Connector.** Connect the appropriate end of Radio Shack's AC Power Supply (***Catalog Number 26-3804***, optional/extra) to this connector. Connect the other end of the power supply to a standard AC wall outlet or approved power strip.

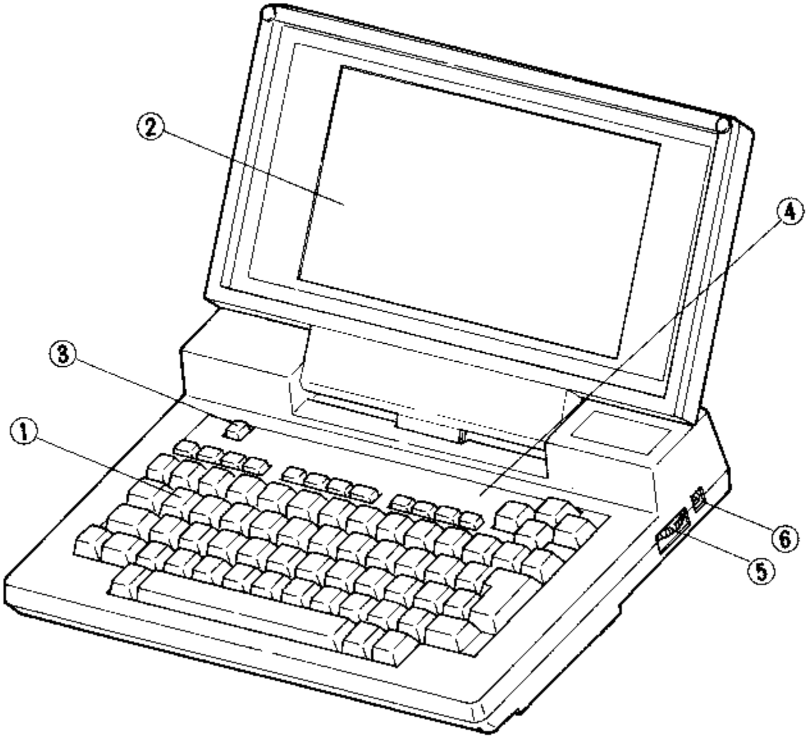


Figure 1. Front View

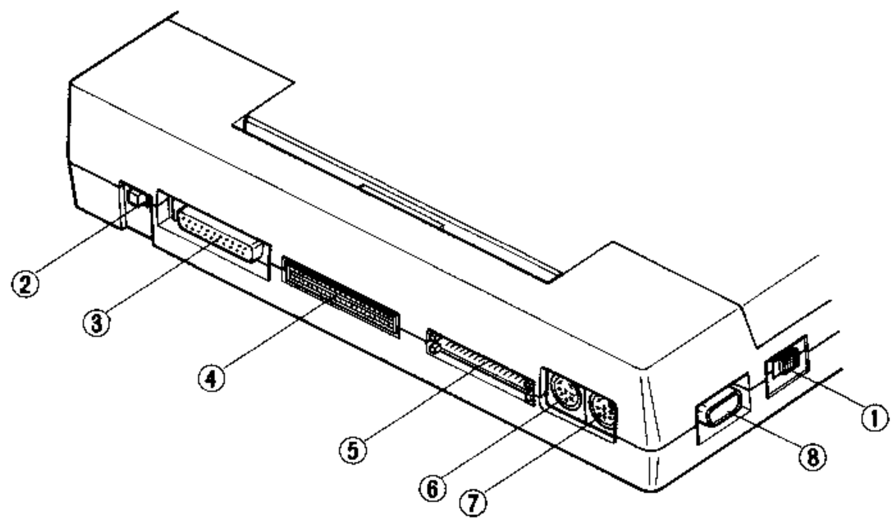


Figure 2. Rear View

1 **DIR/ACP Selector.** This selector allows you to select either a direct or acoustic coupler connection. If you are communicating with another computer over the phone lines via the built-in, direct-connect modem, set this switch to the DIR position. If you are using the optional/extra Model 100 Acoustic Coupler (***26-3805***), set this selector to the ACP position.

2 **RESET Switch.** If the Tandy 200 "locks up" (i.e., the display "freezes" and all keys seem to be inoperative), press this button to return to the Main Menu (start-up). It is not likely that the Tandy 200 will lock-up when you are using the built-in applications programs, however, it may occur with customized programs.

3 **RS-232C Connector.** Attach a DB-25 cable (such as Radio Shack ***Catalog Number 26-1408***) to this connector when you need to receive or transmit serial information. When communicating directly with another Radio Shack computer, a Null MODEM Adapter (***26-1496***) is required. An 8" Cable Extender (***26-1497***) may also be required.

4 **SYSTEM BUS Connector.** Connect this connector to the Disk/Video Interface (***26-3806***), using the system bus cable.

5 **PRINTER Connector.** For hard-copy printouts of information, attach any Radio Shack parallel printer to this connector, using an optional/extra printer cable.

6 **Direct-Connect MODEM (PHONE) Connector.** When communicating with another computer via the Tandy 200's built-in MODEM, connect the round end of the optional/extra modem cable to this connector.

7 **CASSETTE Recorder Connector.** To save or load information on a cassette tape, connect the cassette recorder here. An optional/extra cassette recorder (and cable) is required.

8 **Bar Code Wand Connector.** Attach the optional/extra bar code wand to this connector. Note that special bar code reader software is required.

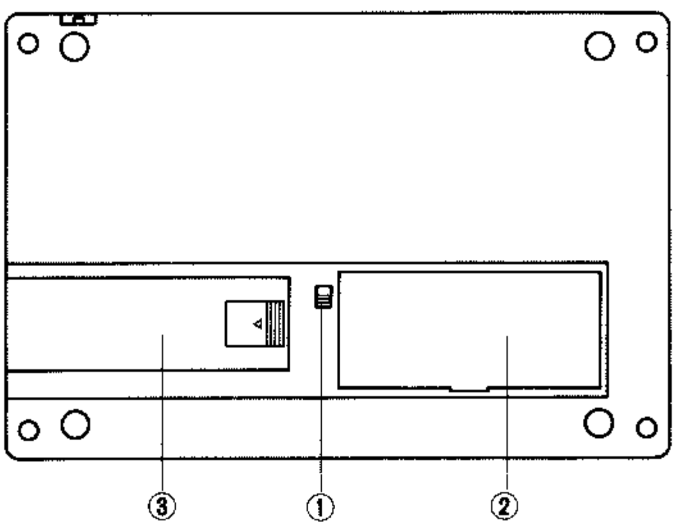


Figure 3. Bottom View

1 **MEMORY POWER Switch.** This switch is used to prevent discharge of the internal Nickel-Cadmium battery, which is used for RAM back-up. The Tandy 200 will operate only when the power switch is set to ON. Set this switch to the OFF position when the Tandy 200 will not be used for a long period of time. Note that the RAM will not be backed up when this switch is set to the OFF position.

2 **Optional ROM and RAM Compartment.** An optional/extra ROM and RAMs can be inserted into this compartment to enhance Tandy 200 capabilities.

3 **Battery compartment.** When not connected to an AC power source, the Tandy 200 gets its power from four AA size batteries that must be installed in this compartment. If the Tandy 200 has the modification jumper module installed Bar Nickel-Cadmium batteries, the battery cover is fixed by a tapping screw and covered by a black sticker.

Internal View

The Tandy 200 consists of four printed circuit boards:

- **LCD PCB**
- **Keyboard PCB**
- **Main PCB**
- **Memory PCB**

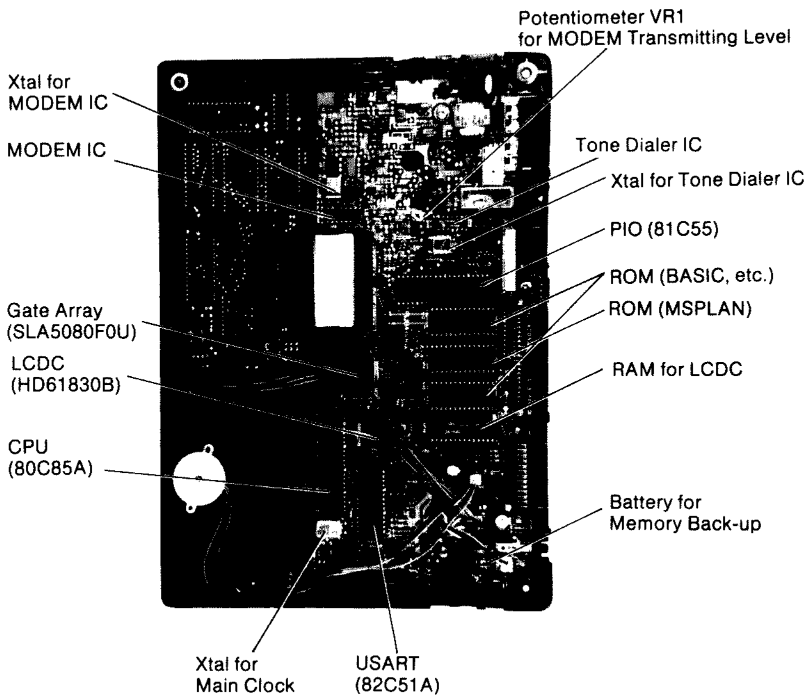


Figure 4. Main PCB

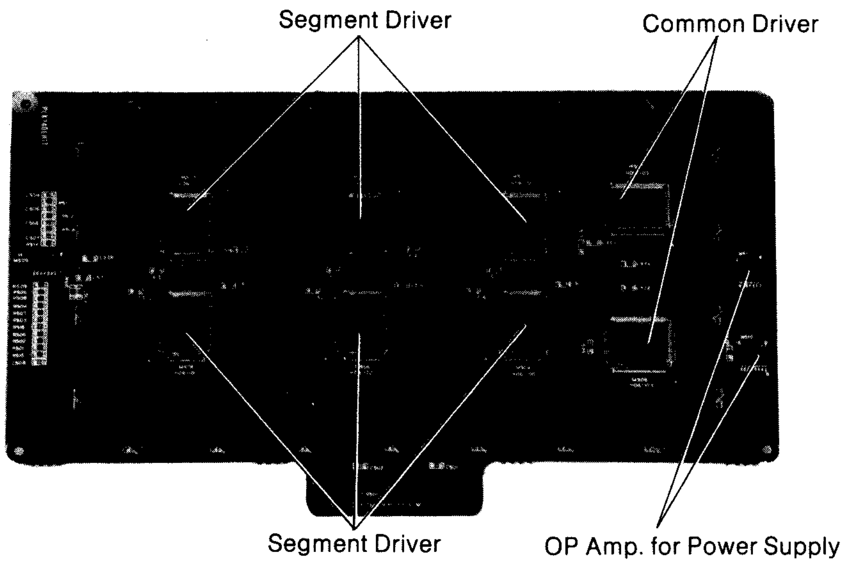


Figure 5. LCD PCB

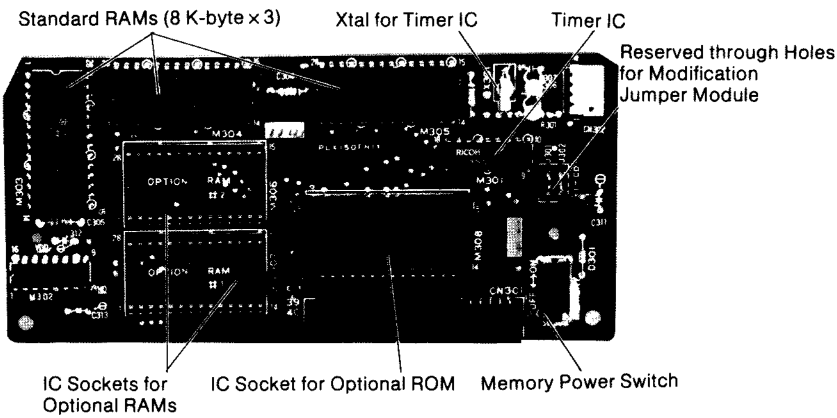


Figure 6. Memory PCB

Specifications

Main Components

Keyboard

71 keys (9×8 matrix)	
Alphabet keys	27
Number keys	10
Picture-control keys	7
Function keys	8
Special symbol keys	8
Mode keys	5
Other special-use keys	6

LCD display

Dot pitch	240×128 full-dot matrix 1/64 duty 1/9 bias
Dot pitch	0.8×0.8 mm
Dot size	0.73×0.73 mm
Effective display area	191.2 (W)×101.6 (D) mm

Operation batteries

Batteries	Four type AA Alkaline-manganese batteries
Operation time	7 days (at two hours/day) (Note: Without I/O units at normal temperature)

Memory protection battery (on Main PCB)

Battery	Rechargeable battery
Back-up time	About 15 days (24 KB) About 5 days (72 KB)
Recharge method	Trickle charge by AC adapter or operation batteries

LSIs

CPU	80C85A Code and pin compatible with 8085
ROM	Maximum 104 KB Standard 72 KB Option 32 KB
RAM	Maximum 72 KB Standard 24 KB RAM Incremental 24 KB RAM on the memory PCB

Dimensions	11-4/5″(L)×8-4/9″(D)×2″(H)
Weight	4 lbs. 4 oz.

I/O Interface

RS-232C

Conforms to EIA Standard Signal

	TXR (Transmit Data) RXR (Receive Data) RTS (Request to Send) CTS (Clear to Send) DSR (Data Set Ready) DTR (Data Terminal Ready)
Communications Protocol	
Word length	6, 7 or 8 bits
Parity	NON, EVEN, ODD or IGNORE
Stop Bit length	1 or 2 bits
Baud rate	75, 110, 300, 600, 1200, 2400, 4800, 9600, 19200 BPS
Maximum transmission distance	5 meters
Drive maximum voltage output	± 5 volts
Drive minimum voltage output	± 3.5 volts
Receive maximum voltage input	± 18 volts
Receive minimum voltage input	± 3 volts

MODEM/Coupler

Conforms to BEL103 Standards

Data length	6, 7 or 8 bits
Parity	NON, EVEN, ODD or IGNORE
Stop bit	1 or 2 bits
Full duplex	Answer mode/originate mode, switchable by software
Other functions	Hang-up function Auto-dialer function

Audio cassette interface

Data Rate	1500 BPS (MARK: 2400 Hz, SPACE: 1200 Hz)

Printer interface

Conforms to Centronics interface standards

Handshake Signal	$\overline{\text{STROBE}}$, BUSY, $\overline{\text{BUSY}}$

THEORY OF OPERATION

General

This section describes the theory of operation for the Tandy 200. Figure 7 shows how this section is organized and highlights significant areas.

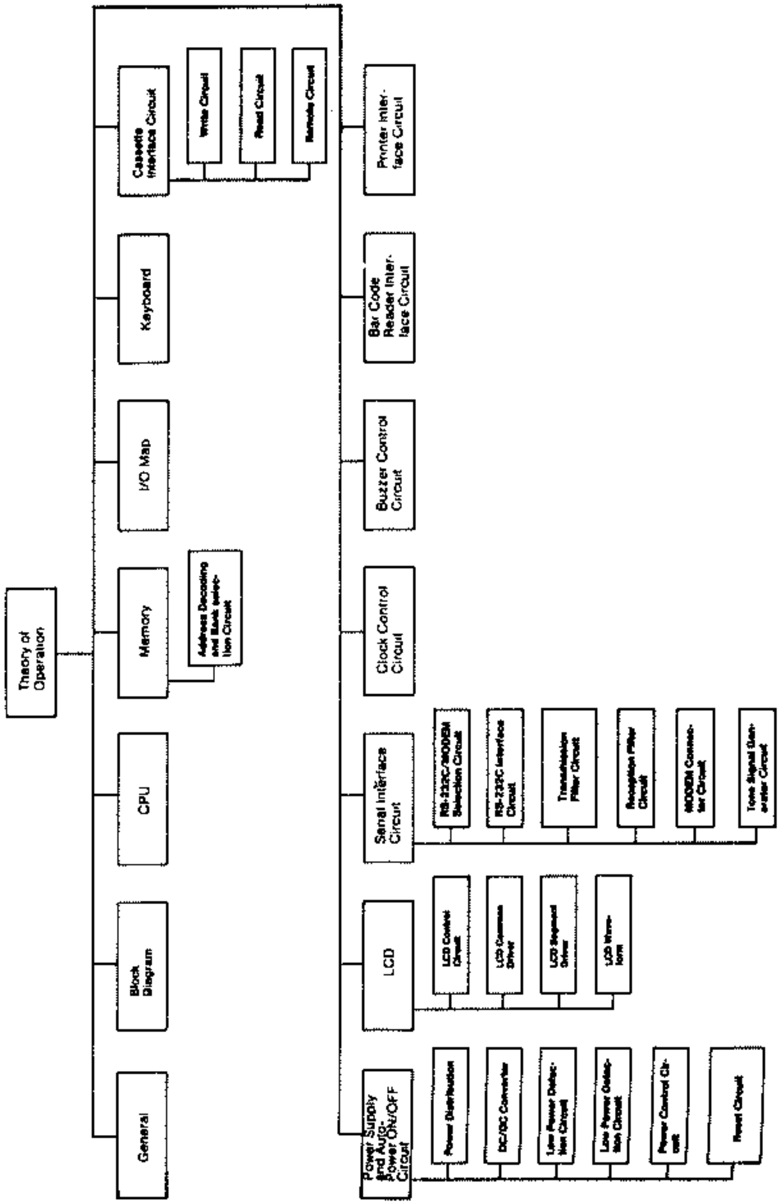


Figure 7. Organization

Block Diagram

The Tandy 200 has four principal LSIs:

- **80C85A CPU**
  This is the Central Processing Unit which controls all functions.
- **81C55 PIO**
  This is the Parallel Input/Output interface controller which controls the printer interface, keyboard, buzzer, clock, LCD interface and data input of BCR interface.
- **82C51A USART**
  This is the Universal Synchronous/Asynchronous Receiver/Transmitter which controls the serial interface such as the RS-232C and MODEM.
- **SLA5080F0U Gate Array**
  This LSI consists of the large number of general-purpose gates which are used for the I/O addressing, bank selection and other control circuits.

The input/output for a cassette recorder and the interruption from the BCR for the starting data are controlled by the CPU directly through its SOD, SID and RST 5.5 terminals.

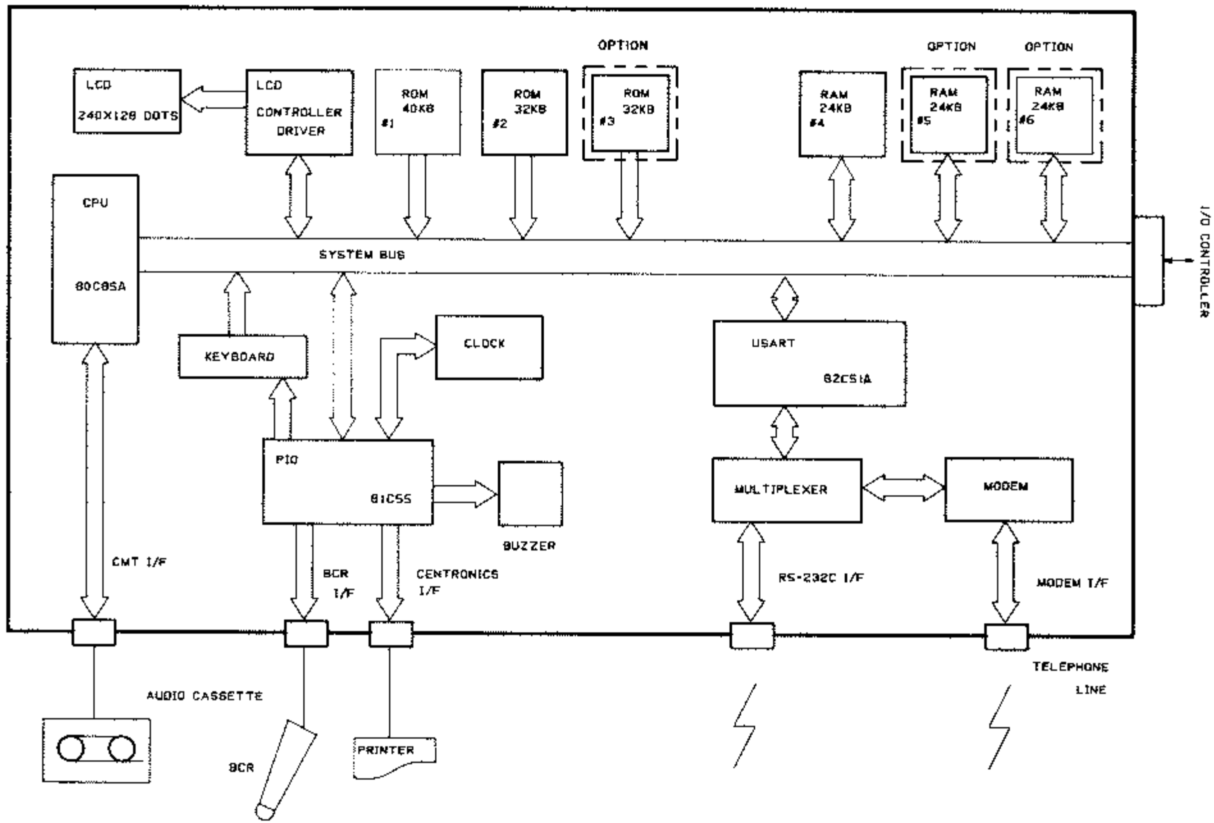


Figure 8. Block Diagram

CPU

The CPU is an 80C85A that runs at a clock speed of 2.4576 MHz. It is an 8-bit, parallel Central Processing Unit using C-MOS technology. The instruction set is fully compatible with the 8085A microprocessor. The 80C85A uses a multiplexed data bus. The CPU bus is divided into two sections — the 8-bit address bus named the A8-A15, and the 8-bit address and data bus named the AD0-AD7. The address and data bus are separated in the SLA5080F0U by using the ALE signal. The functional block diagram of this circuit in the SLA5080F0U is shown in Figure 9.

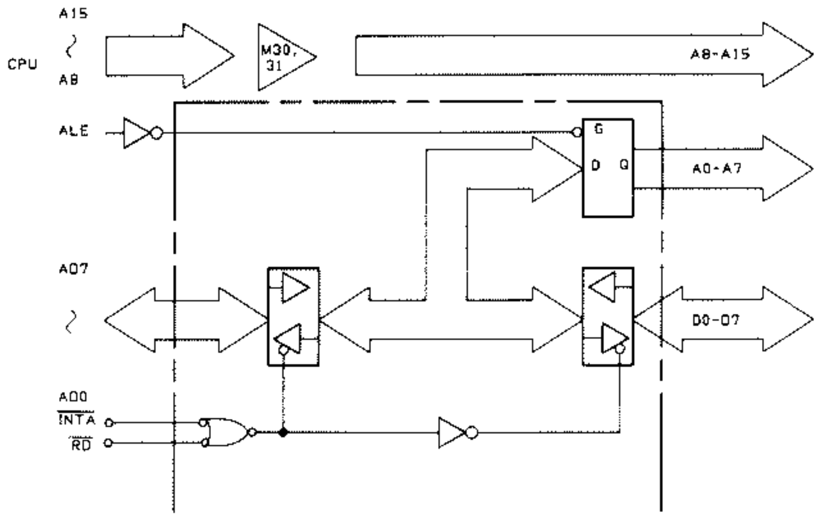


Figure 9. Functional Block Diagram of Bus Separation Circuit

Memory

The Tandy 200 uses a 32K-byte ROM for the MSPLAN, 40K-byte ROM for BASIC and the other application programs, and 24K-byte static RAM to store the data and programs. The 40K-byte ROM consists of an 8K-byte ROM (M13) and 32K-byte ROM (M15). The 24K-byte RAM consists of three 8K-byte RAMs.

Furthermore, a 32K-byte ROM and two 24K-byte RAM packages can be used optionally. The 24K-byte RAM package consists of three 8K-byte RAMs and one decoder IC (40H138), mounted on a ceramic substrate.

Figure 10 shows the memory map and Figure 11 shows the internal wiring diagram of the RAM package.

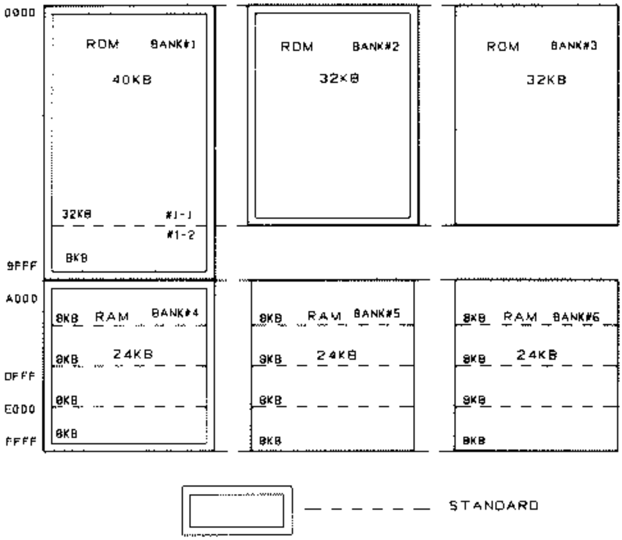


Figure 10. Memory Map

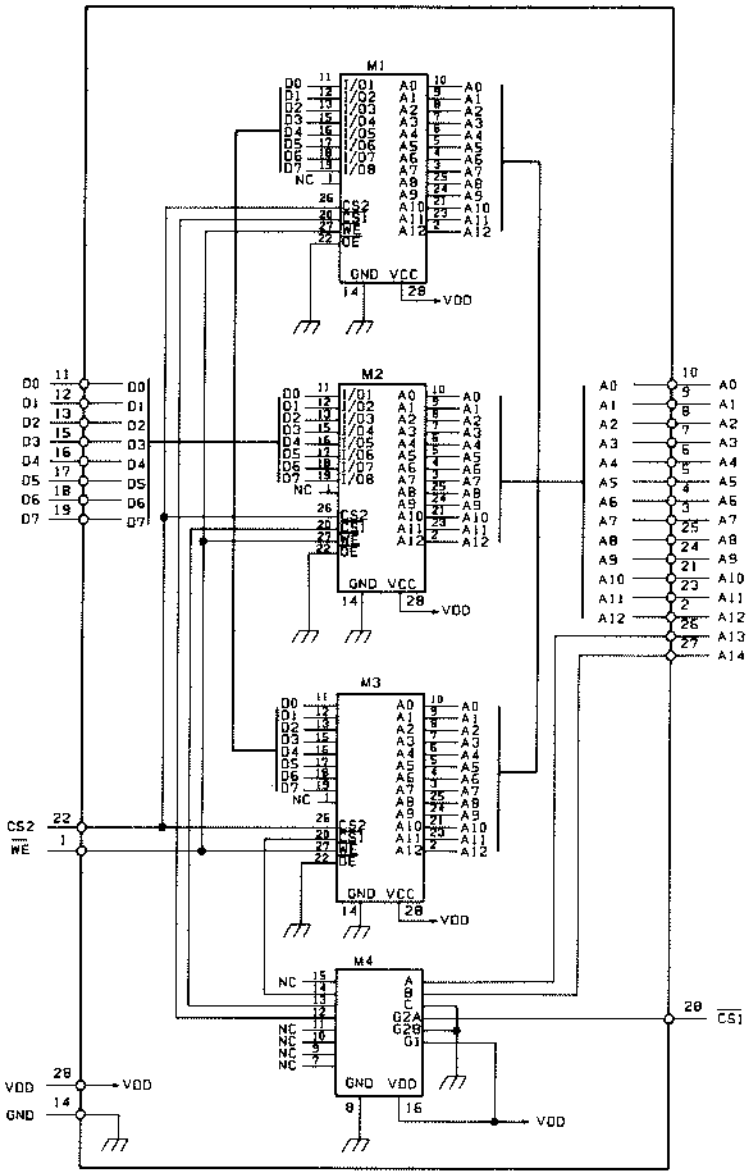


Figure 11. Internal Wiring diagram of RAM package

Address Decoding and Bank Selection Circuit

Selection of RAMs and ROMs are determined by the address and bank signals generated in the SLA5080F0U.

Figure 12 shows the bank selection circuit in the SLA5080F0U.

The latch AA0036 stores the bank selection data sent from the CPU with the $\overline{Y5}$ and $\overline{WR}$ signal. The decoder AA0038 is enabled by the memory address 0000H to 9FFFH for ROMs and the decoder AA0037 is enabled by the memory address A000H to FFFFH for RAMs.

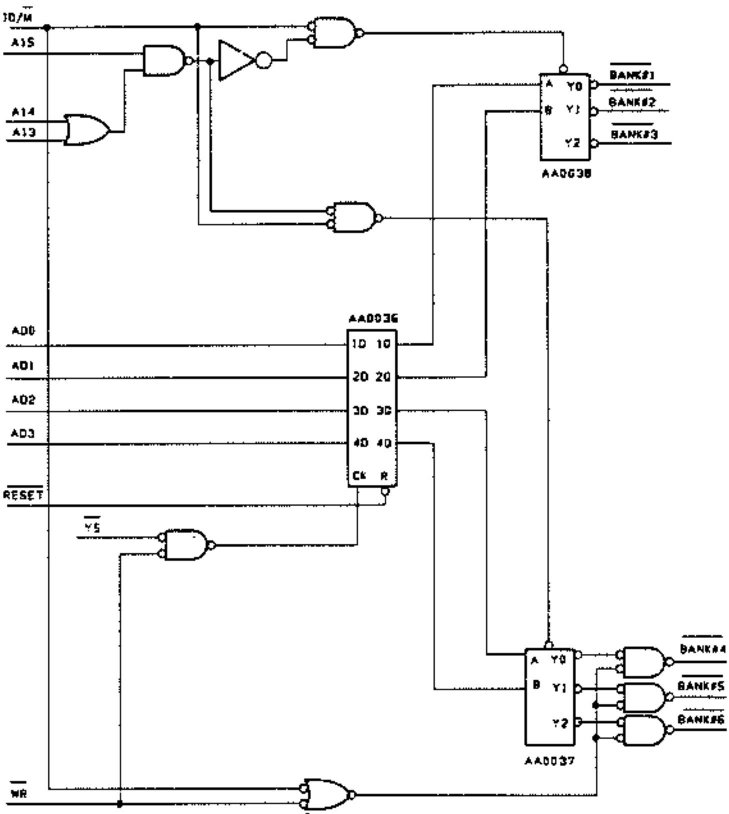


Figure 12. Bank Selection Circuit

I/O Map

Figure 13 shows the I/O address decoding circuit included in the SLA5080F0U that decodes address signals AD4-AD6. The AD7 signal acts as the enable signal for the decoder AA0024 with the IO/$\overline{M}$ signal. At the latch AA0063, the chip enable terminals $\overline{G1}$ and $\overline{G2}$ are connected to the ALE signal passing through the inverter, because the AD0-AD7 signals are the multiplexed bus.

The I/O map and I/O port description are shown in Figure 14.

The port assignment of the 81C55 is shown in Table 1.

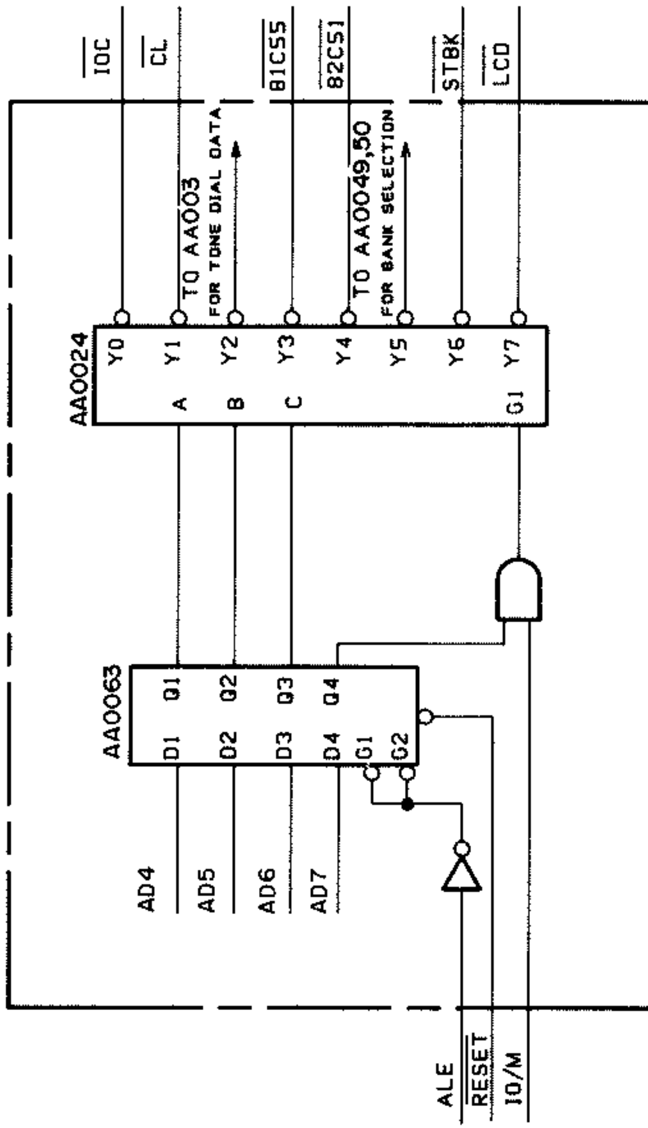


Figure 13. I/O Address Decoding Circuit

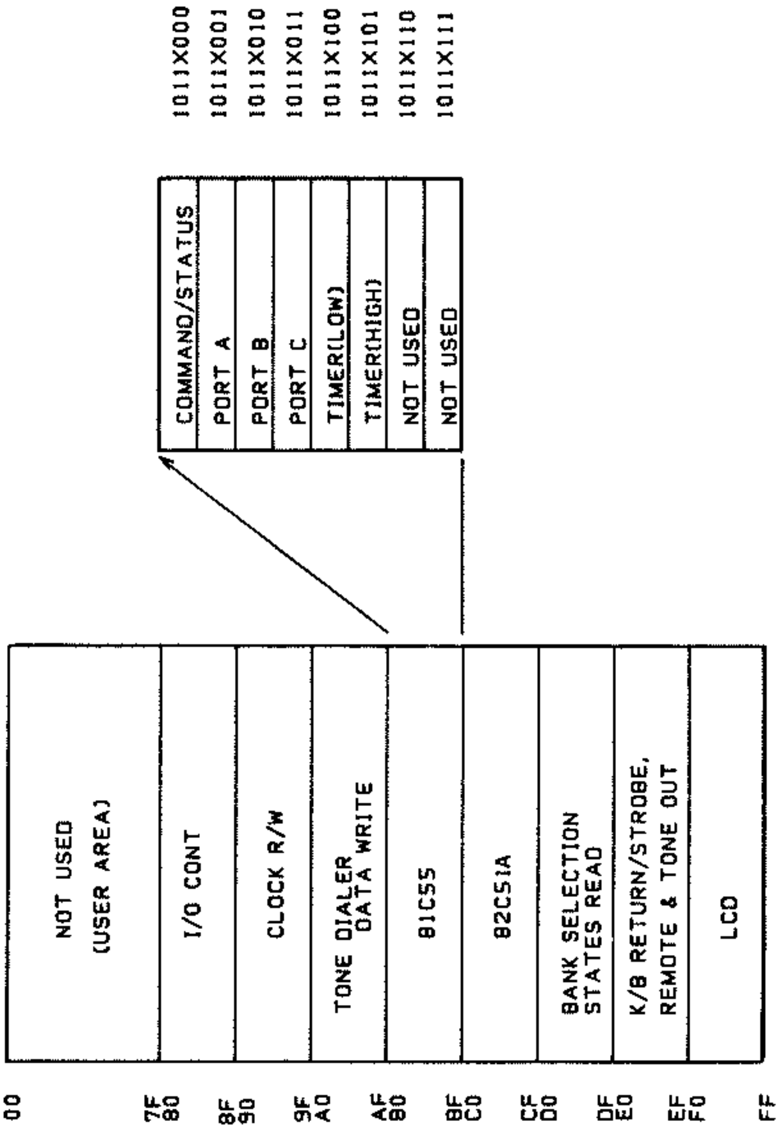


Figure 14. I/O Map and I/O Port Description

Port Assignment of 81C55

Terminal	I/O	Description
PA0	O	Print Data 0, Key Scan 0
PA1	O	Print Data 1, Key Scan 1
PA2	O	Print Data 2, Key Scan 2
PA3	O	Print Data 3, Key Scan 3
PA4	O	Print Data 4, Key Scan 4
PA5	O	Print Data 5, Key Scan 5
PA6	O	Print Data 6, Key Scan 6
PA7	O	Print Data 7, Key Scan 7
PB0	O	Print Data 8, Key Scan 8
PB1	O	ORIG/ANS Output ("H" = ORIG, "L" = ANS)
PB2	O	BUZZER Output (Active "L")
PB3	O	$\overline{\text{RS232C}}$ ("H" = Modem select, "L" = RS-232C select)
PB4	O	Power Cut Signal (PCS) Output (Active "H")
PB5	O	BELL Output
PB6	O	Modem Enable (MEN) Output (Active "H")
PB7	O	CALL Output (Active "H") Connects and disconnects the telephone line.
PC0	I	Low Power Sence ($\overline{\text{LPS}}$) Input (Active "L")
PC1	I	$\overline{\text{BUSY}}$ Input (Active "L")
PC2	I	BUSY Input (Active "H")
PC3	I	BCR Data Input (black line = "H", white line = "L")
PC4	I	Carrier Detect (CD) Input
PC5	I	Carrier Detect Break Down (CDBD) Input (Active "H")
TO	O	Clock Output and Melody Output for 82C51A (USART)

Table 1. Port Assignment of the 81C55

Keyboard

Key strobe signals are emitted from the PB0 and PA0-PA7 terminals of the 81C55, and the return signals from the keyboard pass through the octal bus buffer (M27) which is enabled by NANDing the $\overline{RD}$ and $\overline{STB/K}$ signals at M29, and then the return signals are sent to the CPU.

The $\overline{STB/K}$ signal is generated in the SLA5080F0U when the CPU assigns EO-EFH to the I/O port address. The CPU starts the key scan operation when the RST 7.5 interruption is accepted. This interruption (TP signal) is generated about every 3.3 msec. at M34 by dividing the CLK signal (2.4576 MHz).

Condition of pressing "T" key is shown in Figure 15.

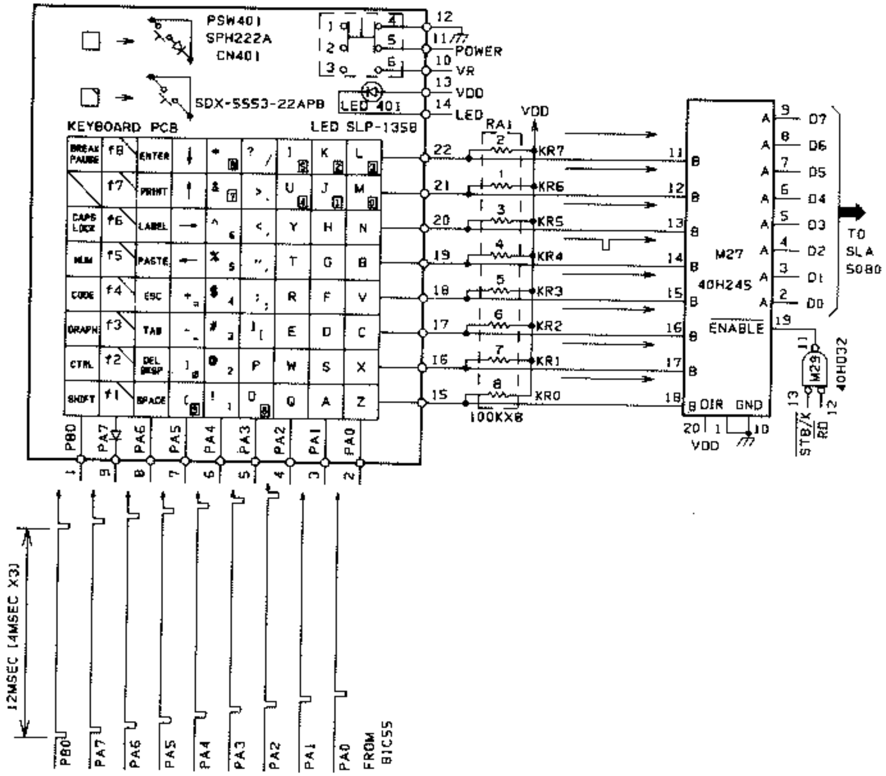


Figure 15. Condition of Pressing "T" Key

Cassette Interface Circuit

The cassette interface circuit is subdivided into three sections:

- **Write Circuit**
- **Read Circuit**
- **Remote Circuit**

Write Circuit

The write circuit is accomplished in several steps. First, the serial data from the SOD terminal of the CPU is inverted by M1. Then, the DC component is removed by C3. And finally, the data passes through an integrator consisting of R8 and C2, and after voltage division, out to a cassette recorder AUX jack.

Figure 16 shows the write circuit of the cassette interface.

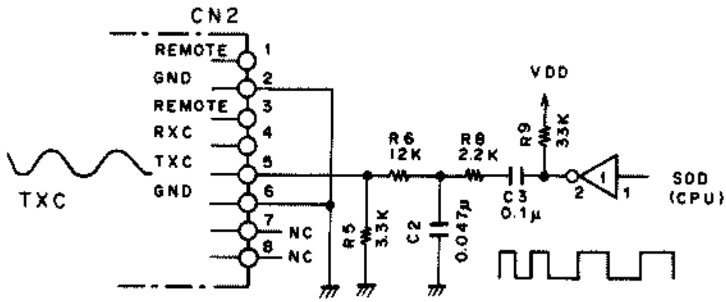


Figure 16. Write Circuit of Cassette Interface

Read Circuit

The signal input from the earphone jack of the cassette recorder passes through the clamp circuit consisting of D1 and D2, and then is input to the comparator circuit consisting of M2.

Finally, the signal is converted into the digital signal and sent to the SID terminal of the CPU. Figure 17 shows the read circuit.

In the circuit, D8 clamps the negative voltage output of the comparator.

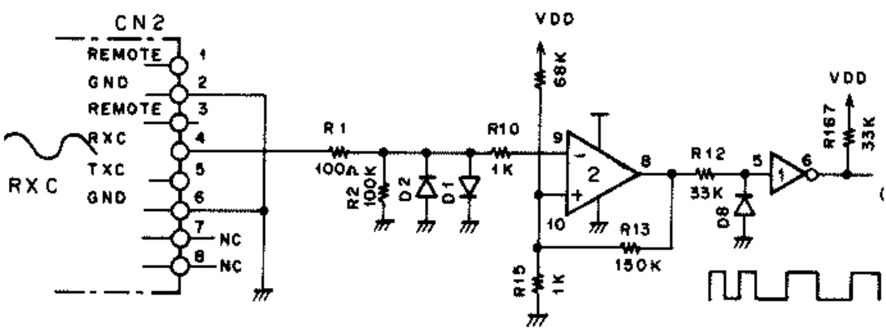


Figure 17. Read Circuit of Cassette Interface

Remote Circuit

By writing-in data "1" into bit 1 of the output port specified by E0-EFH, the REMOTE terminal of the SLA5080F0U is changed to "H." Then T11 is switched ON and RY1 is energized. This controls the motor of the cassette recorder.

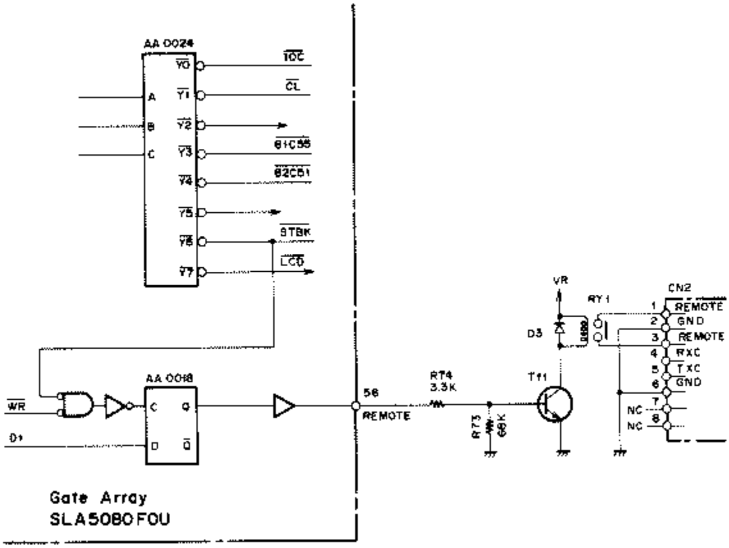


Figure 18. Remote Circuit of Cassette Interface

Printer Interface Circuit

The printer interface circuit conforms to Centronics standards. As shown in Figure 19, the BUSY signal from the printer is read from the PC2 of the 81C55. If the condition is not busy (PC2 = "L"), the 8-bit parallel data (PA0-PA7 from 81C55) is sent to the printer. Then, by writing-in data "1" into bit 1 of the output port specified by I/O address E0-EFH, the PSTB signal is generated in the SLA5080F0U and sent to the printer.

As soon as the printer receives this PSTB signal, the BUSY signal is changed to "H" indicating that the printer is busy. The CPU then waits for a while until this BUSY signal becomes "L." As soon as the printer prints the one character specified by the 8-bit parallel data, the BUSY signal becomes "L." Then, the CPU sends the next 8-bit parallel data.

If the printer is in ON LINE condition, the BUSY signal is "H" and sent to the CPU, passing through the PC1 of the 81C55. But, when in the OFF LINE condition, the BUSY signal is "L" and transmission of print data to the printer is inhibited by the CPU.

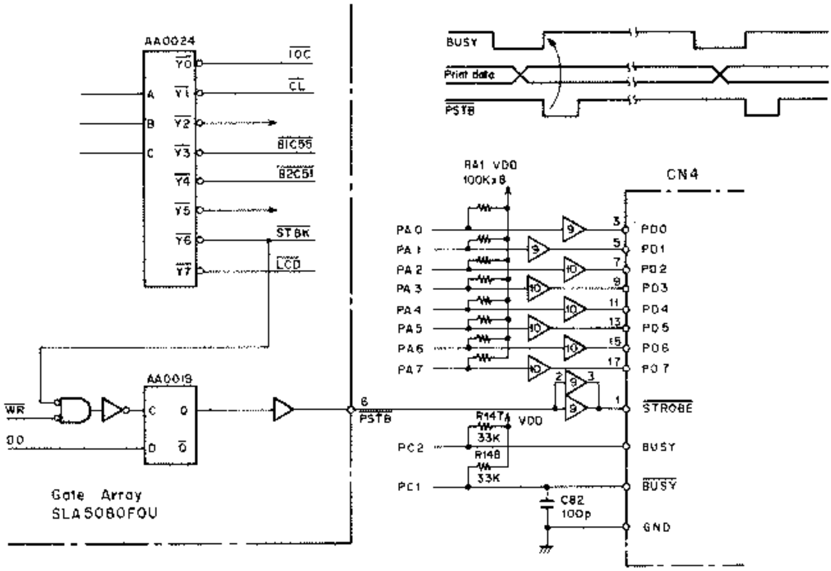


Figure 19. Printer Interface Circuit

Bar Code Reader Interface Circuit

The input signal from the bar code reader is subjected to waveform shaping, inverted by the Schmitt-type inverter (M1), and then sent to the PC3 terminal of the 81C55 and the RST 5.5 terminal of the CPU.

When the bar code reader reads the first white part of the bar code, a "L" level signal is generated, then inverted by M1. As soon as RST 5.5 interruption occurs, the CPU starts the data input operation, passing through the PC3 of the 81C55. As the bar code reader is moved across the bars, "H" and "L" signals (which correspond to white and black bars respectively) are generated continuously and inversion signals are sent to the PC3 of the 81C55 as the serial input data. Refer to Figure 20.

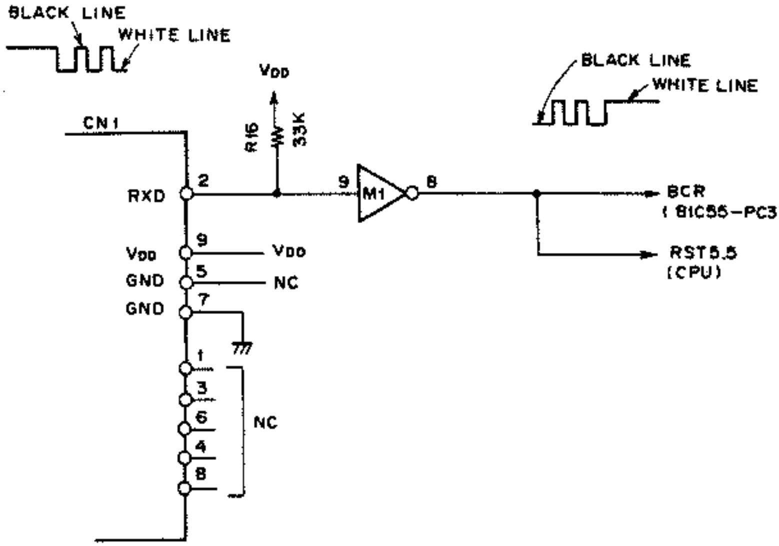


Figure 20. Bar Code Reader Interface Circuit

Buzzer Control Circuit

There are two ways to operate the buzzer. One is to sound the buzzer with the specified frequency by emitting a signal from the PB5 terminal of the 81C55 and the other, by using timer output (TO) and the BUZZER signal (PB2) of the 81C55. In addition, the BELL signal also acts as the control signal of the DC/DC converter circuit during the power-up sequence (refer to the Power Control Circuit).

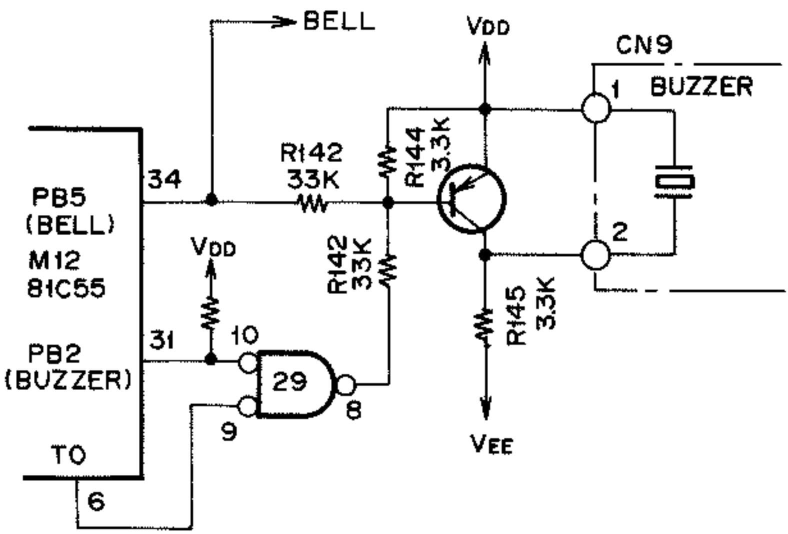


Figure 21. Buzzer Control Circuit

Signal from the PB5 of the 81C55

When the PB2 of the 81C55 is "H," the buzzer sounds by repeated switching of the buzzer driving transistor. This is caused by "H", "L", "H", "L" . . . output signals from the PB5 synchronizing with the frequency for sounding the buzzer. This method is used for the BEEP command in BASIC.

Using the 81C55 Timer Output

In this method, the buzzer is made to sound by setting the 81C55 timer in the square wave output mode. To write the value corresponding to the sound frequency, the CPU assigns B4, B5, BC or BD to the I/O port address. This frequency is assigned by the first parameter of the SOUND command in BASIC.

If the above procedures are completed, the TO terminal of 81C55 outputs the square waves, and the PB2 of the 81C55 controls the length of the sound whenever the PB5 is "L." How long the sound is heard depends on the second parameter of SOUND command in BASIC.

Clock Control Circuit

A TIMER IC (RP5C01) on the memory PCB is used in the clock control circuit so that the current time and alarm time can be set and read by the commands in BASIC.

To set and read the time, the CPU assigns 90-9FH to the I/O port address.

In addition, because the back-up power VB is supplied to the TIMER IC, the clock and alarm functions are enabled even when the Tandy 200 is in the power-off condition.

Figure 22 shows the internal block diagram, and Table 2 shows the I/O port address assignment of each function. An internal 26×4-bit RAM is used as a buffer memory when the data is transmitted between RAM banks.

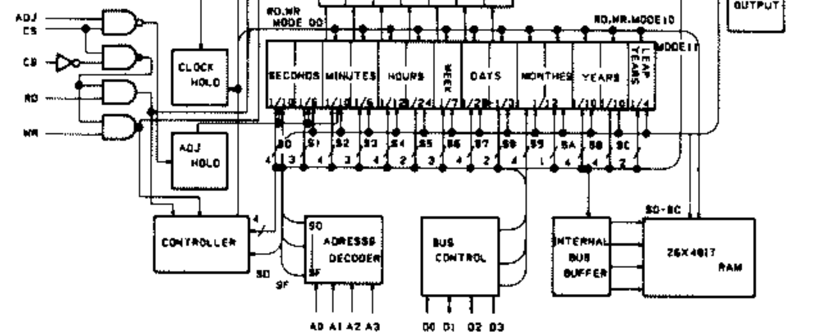


Figure 22. RP5C01 Internal Block Diagram

Address Assignment of RP5C01

MODE	MODE 00					MODE 01					10	11
A3 ~ A0	Description	D3	D2	D1	D0	Description	D3	D2	D1	D0	Description	
0	One sec. Counter						×	×	×	×		
1	Ten sec. Counter	×					×	×	×	×		
2	One min. Counter					Alarm One sec. Register					10	11
3	Ten min. Counter	×				Alarm Ten min. Register	×					
4	One hour Counter					Alarm One hour Register						
5	Ten hours Counter	×	×			Alarm Ten hours Register	×	×			4bit	4bit
6	Day Counter	×				Alarm Day Register	×				×	×
7	One day Counter					Alarm One day Register					13	13
8	Ten days Counter	×	×			Alarm Ten days Register	×	×				
9	One month Counter						×	×	×	×	RAM	RAM
A	Ten month Counter	×	×	×		12/24 Hours Selector	×	×	×			
B	One year Counter					Leap Year Counter	×	×				
C	Ten years Counter						×	×	×	×		
D	Mode Register	Timer EN	Alarm EN	M1	M0		Timer EN	Alarm EN	M1	M0	←	←
E	Test Register	Test 3	Test 2	Test 1	Test 0		Test 3	Test 2	Test 1	Test 0	←	←
F	Reset Controller etc.	1 Hz ON	16 Hz ON	Timer Reset	Alarm Reset		1 Hz ON	16 Hz ON	Timer Reset	Alarm Reset		

x: Don't care when writing, always "0" when reading.

Table 2. RP5C01 I/O Port Address Assignment

To set and read the time and alarm information, the CPU proceeds in the following sequence.

Write or Read the timer

X: Don't care

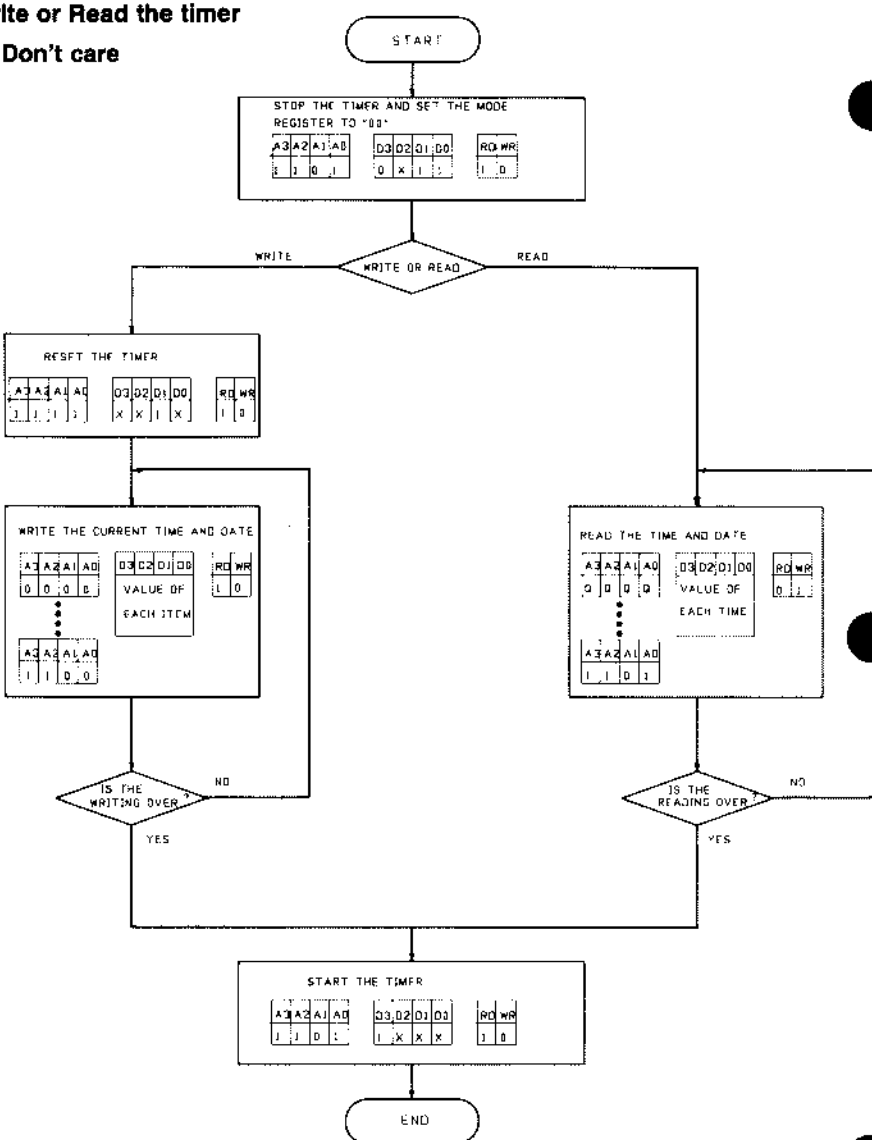


Figure 23. Flowchart for the TIMER IC

Write or Read the alarm time

X: Don't care

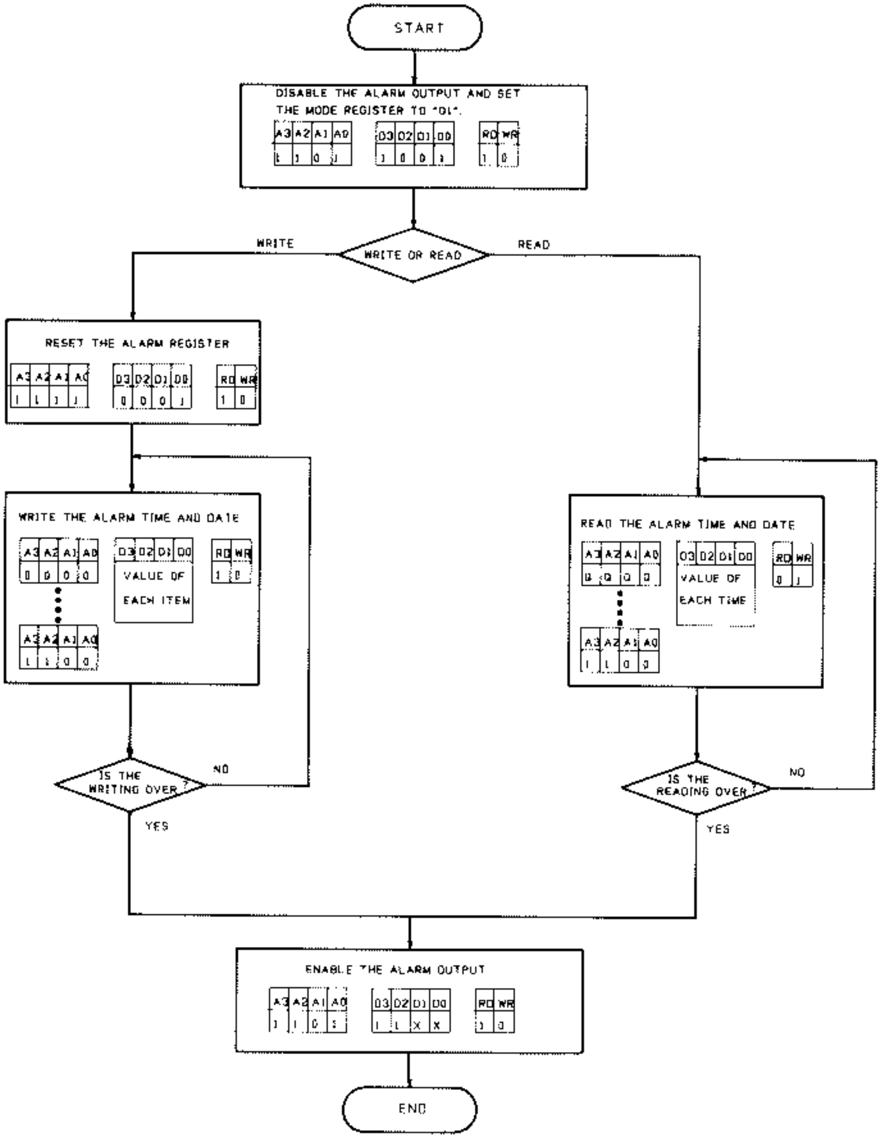


Figure 23. Flowchart for the TIMER IC

(continued)

Serial Interface Circuit

The serial interface circuit supports asynchronous serial transmission/reception.

The heart of this circuit is the 82C51A (USART). It performs the job of converting the parallel byte data from the CPU to a serial data stream including start, stop and parity bits.

For a more detailed description of how this IC performs these functions, refer to Appendix C of this manula.

Figure 24 shows the functional block diagram of the serial interface circuit. In this figure, the TO signal, basic timing clock for the USART, defines the transmission/reception baud rate.

To transmit and receive the serial data from external devices, the $\overline{\text{RS232C}}$ signal selects either MODEM or RS-232C interface. During the MODEM operation, the ORGIS signal switches either the originate mode or answer mode for the MODEM IC.

The serial interface circuit is subdivided into the following circuits:

- **RS-232C/MODEM Selection Circuit**
- **RS-232C Interface Circuit**
- **MODEM IC**
- **Transmission Filter Circuit**
- **Reception Filter circuit**
- **MODEM Connector Circuit**
- **Tone Signal Generator Circuit**

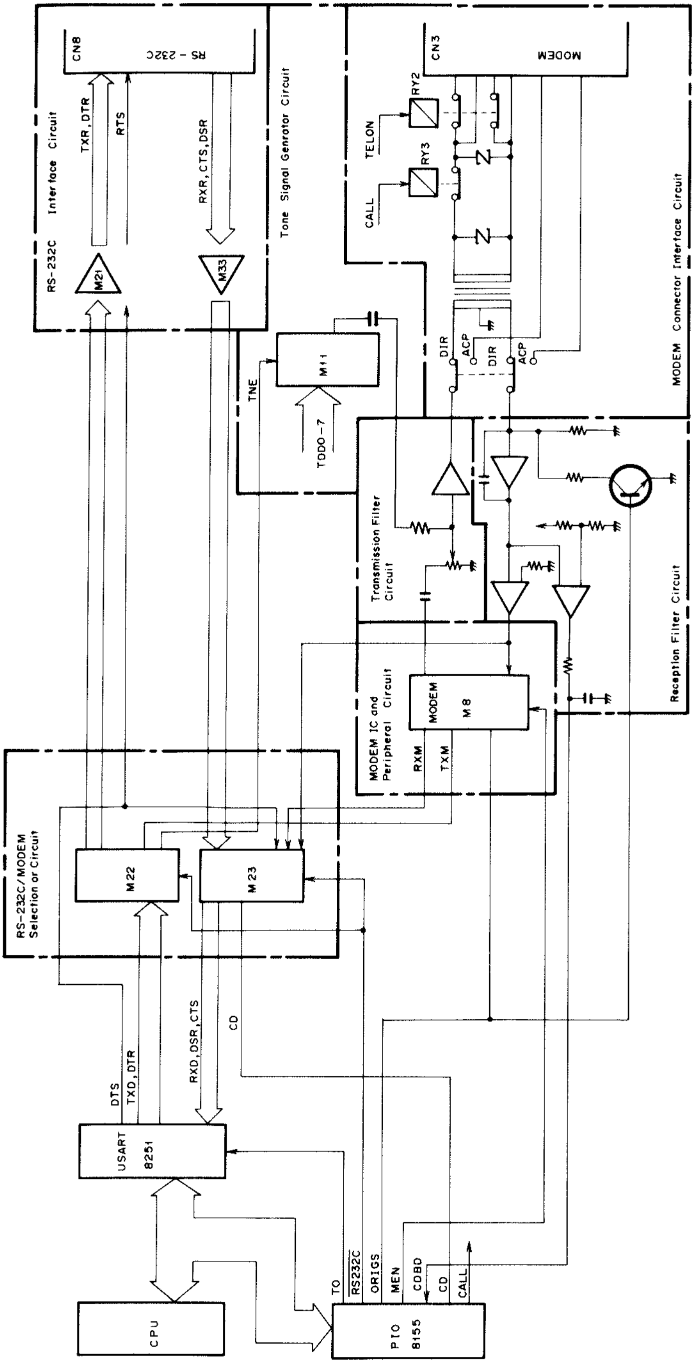


Figure 24. Functional Block Diagram of the Serial Interface

RS-232C/MODEM Selection Circuit

The $\overline{\text{RS232C}}$ signal (PB3 terminal of the 81C55) determines whether the serial port is to be used as RS-232C or as MODEM. When the $\overline{\text{RS232C}}$ signal is "L," the serial port is used as RS-232C. When the $\overline{\text{RS232C}}$ signal is "H," the port is used as MODEM.

The reception signal, including the control signal, is demultiplexed at M23. The transmission signal is multiplexed at M22.

During the RS-232C mode, the CD (Carrier Detect) signal is not used. To make this condition, pin 14 of M23 is connected to the ground.

During the MODEM mode, the RTS signal is used as the self-loopback signal and it is sent back to the CTS terminal. The DSR signal is not used in the Tandy 200 USA version, since the TD signal is always fixed to "H" level by the hardware. The CD signal selects the CDD signal from the RXCAR terminal of the MODEM IC. Because the CPU detects the carrier signal by counting the frequency of the CDD signal corresponding with the originate mode or answer mode. When a customer uses the tone dialer function, the DTR signal acts as the enable signal for the tone dialer IC.

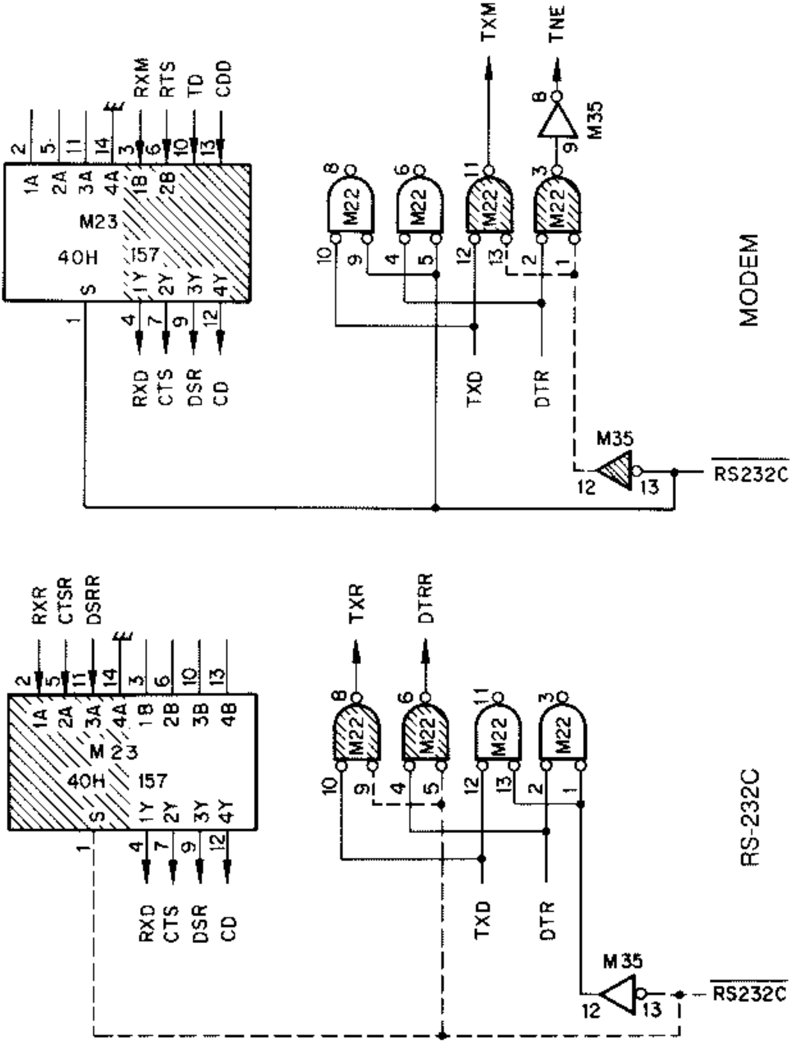


Figure 25. RS-232C/MODEM Selection Circuit

RS-232C Interface Circuit

In the RS-232C transmission circuit, after the DC component is removed from the signals by the coupling capacitors, the signals are leveled to ±5V signals by the inverters connected in parallel, and then are output as RS-232C transmission signals. In the RS-232C reception circuit, the DSRR, CTSR, and RXR signals from the external RS-232C line are subjected to waveform shaping and inverted by M33, and then converted to +5V or ground level signals by the diodes. The signals are then demultiplexed at M23 and converted to CTS, DSR and RXD signals which are input to the 82C51A. The CD signal is not used in the Tandy 200.

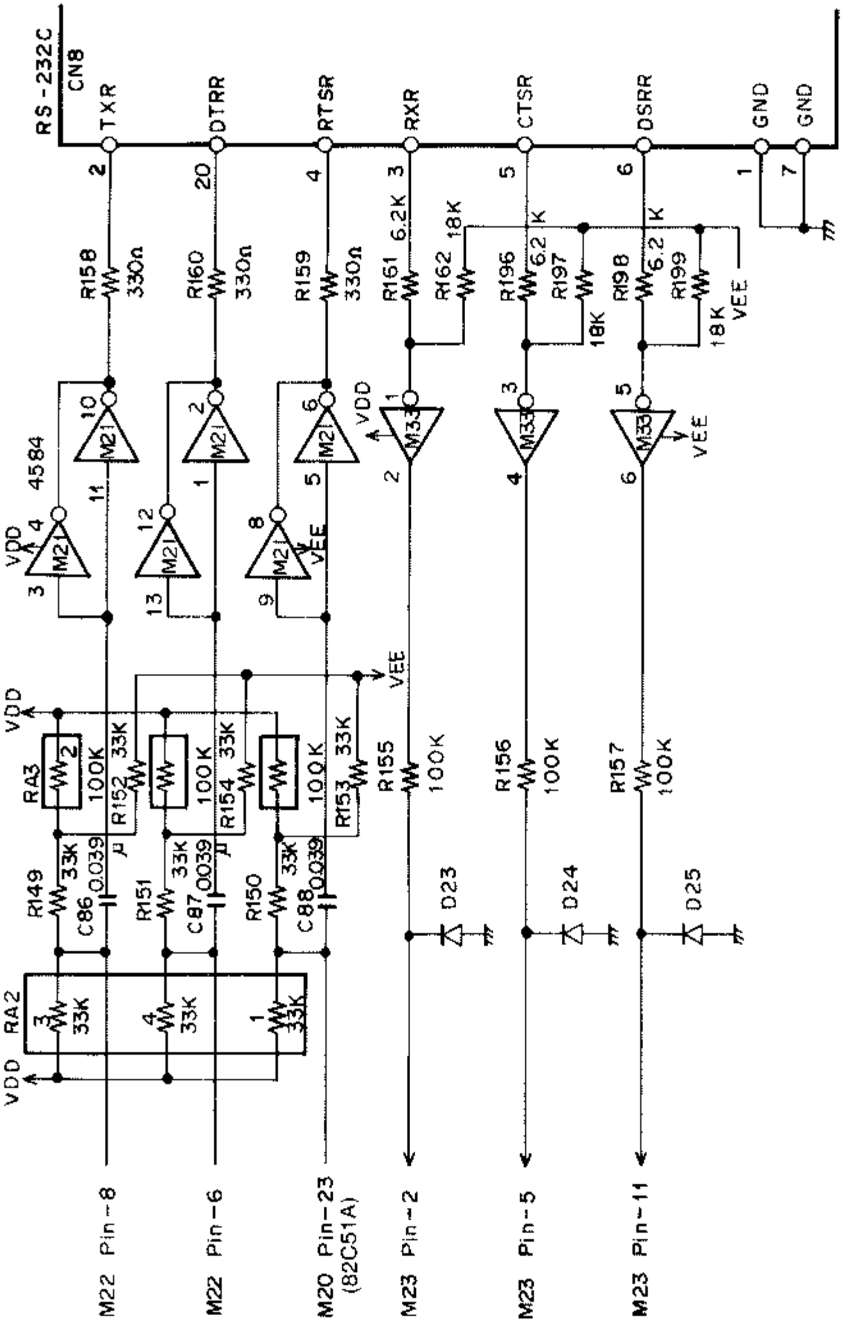


Figure 26. RS-232C Interface Circuit

MODEM IC

The Tandy 200 employs the IC MC14412 as a MODEM control device. This IC modulates/demodulates data to be transmitted/received in accordance with frequencies suitable for originate or answer mode respectively.

The RXRATE and TYPE terminals of MC14412 (M8) are pulled up to VDD.

The baud rate is set to 300 bps, and the U.S. Standard is selected. Since the ECHO and SELF TEST terminals are not needed, they are connected to ground.

The PB6 terminal of the 81C55 outputs the enable signal (MEN) for the MODEM IC until the unit is in the MODEM mode.

In addition, the signal designated by the ORIG-ANS parameter in TELCOM mode is input to MODE input terminal, and it switches between the originate mode or the answer mode. This signal is output from the PB1 terminal of the 81C55.

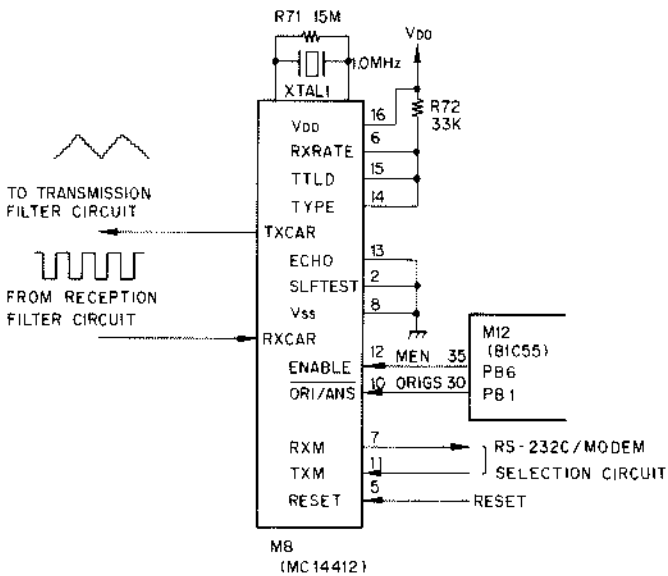


Figure 27. MODEM IC and Peripheral Circuit

Transmission Filter Circuit

The DC component of the carrier output from the TXCAR terminal is removed by C50. The signal level is adjusted by the potentiometer VR1. The signal then passes through the transmission band-pass filter and is sent to the telephone line or the acoustic coupler.

The transmission filter circuit is composed of an active filter (consisting of an operation amplifier) and the intermediate frequency of the active filter is 1200 Hz which covers both originate mode and the answer mode.

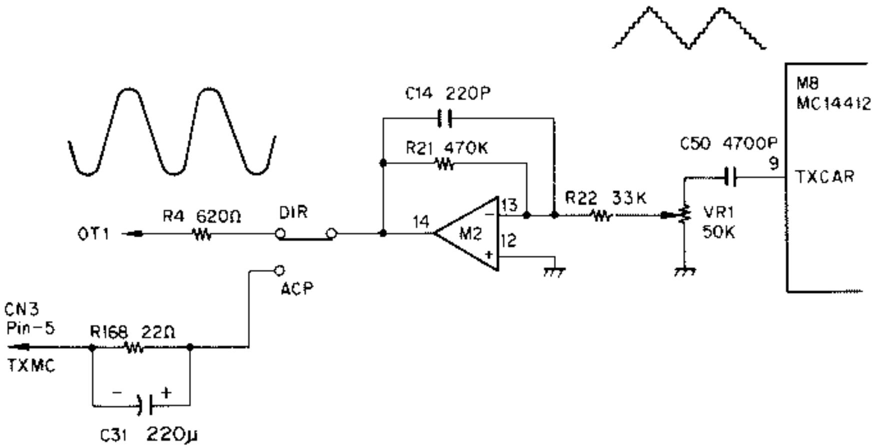


Figure 28. Transmission Filter Circuit

Reception Filter Circuit

As shown in Figure 29, the reception input signal is amplified when passing through coupling capacitor (C11), and amplified again as it passes through the 3-stage band-pass filter (composed of an active filter). The signal then passes through the comparator, and after being changed to a square wave, is input at the RXCAR terminal of MC14412. Also, to check a carrier signal, this signal is input to the demultiplexer M23 as the CDD signal in the RS-232C interface circuit.

Intermediate frequencies of the 3-stage active filter are shown below. The switching of intermediate frequency for the originate and answer modes is accomplished by switching T1, T2 and T3 ON or OFF according to ORIG-ANS parameter in TELCOM mode, thus changing the input resistance of the filters.

On the other hand, three comparators consisting of M5 act as the carrier break down detector. The output of this circuit is "H" when a carrier signal has not been detected for the time specified by the C38 and R66.

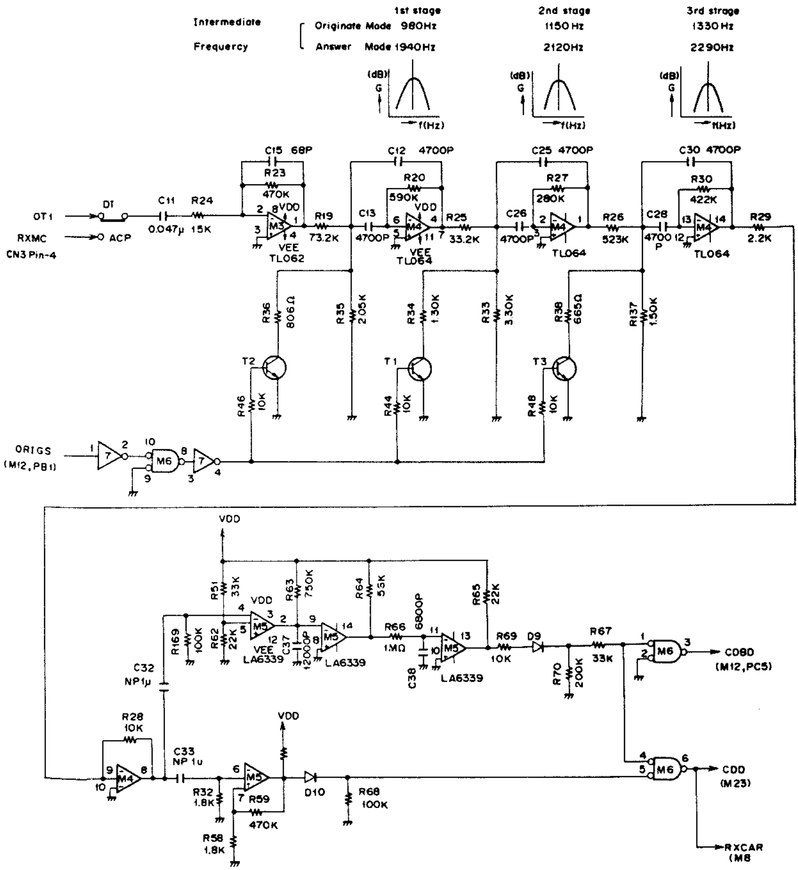


Figure 29. Reception Filter Circuit

MODEM Connector Interface Circuit

When the acoustic coupler is used, the transmission and reception signals are directly connected to the connector (TXMC, RXMC). When the MODEM cable is used, they are connected to the secondary side of the driver transformer. The primary side of this transformer is connected to the telephone line via the connector (TXMD, RXMD).

The ACP-DIR switch is used in the MODEM mode, relay RY2 separates the telephone receiver audio inut signal (TL) to prevent interference. RY3, another relay, separates the modem circuit and the telephone at the conclusion of use in the MODEM mode and is also used as an automatic dialer for the pulse type telephone line.

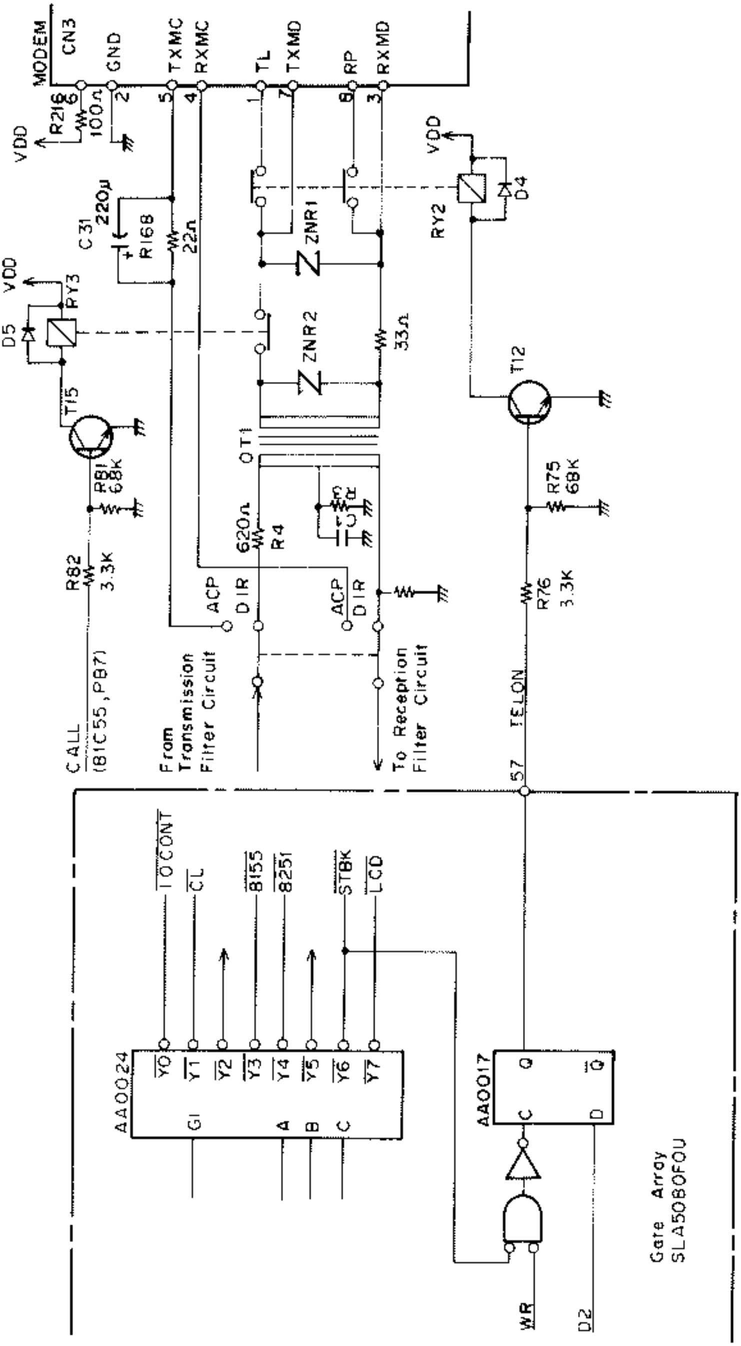


Figure 30. MODEM Connector Interface Circuit

Tone Signal Generator Circuit

The function of this circuit is to send tone-dial signals to the tone-type telephone line when the Tandy 200 is connected to that type of telephone line.

These functions described above are controlled by the IC TCM5089. The enable (TNE) signal input to this IC is created by NANDing the DTR signal and RS232C signal. That is, when the DTR signal becomes "H" during MODEM mode, this IC will be in the enable state.

Then the CPU writes the data to be dialed to the I/O port assigned by A0H – AFH.

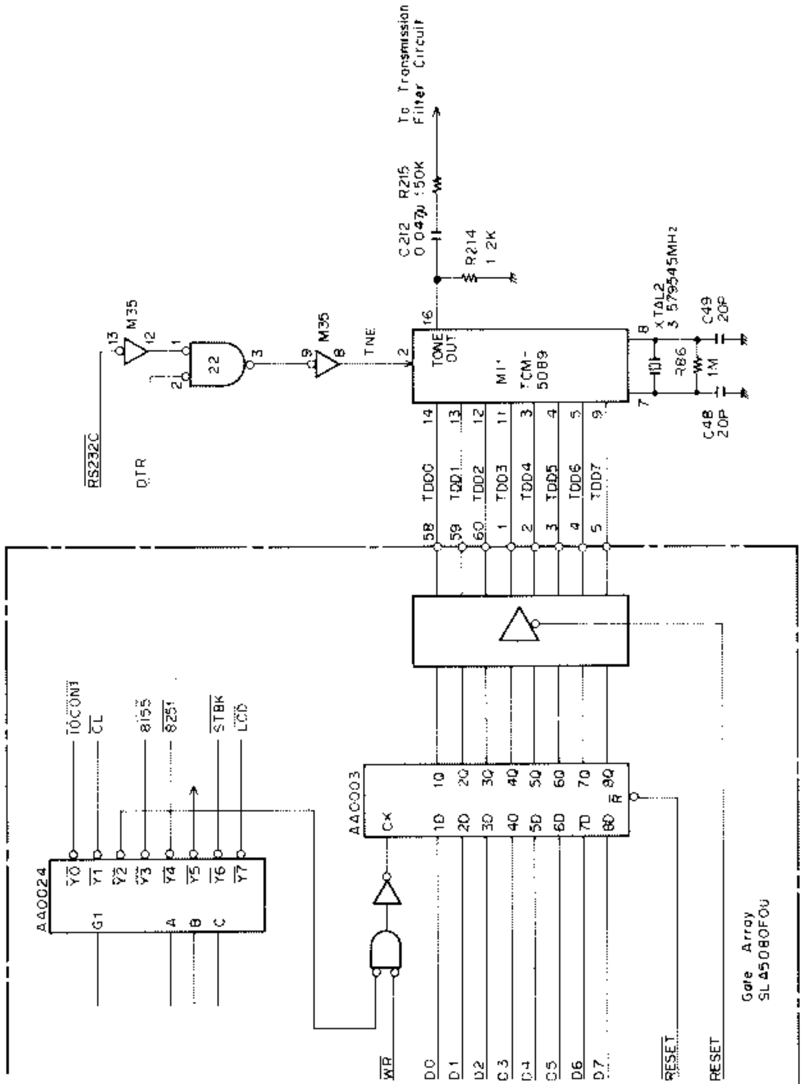


Figure 31. Tone Signal Generator Circuit

LCD

The LCD used in the Tandy 200 is composed of electrodes in a matrix arrangement (128 common signals and 480 segment signals).

Because this LCD operates on a 1/64-duty time division drive, the upper 64 and lower 64 common signals are performed by the same timing.

This part is subdivided into following four sections:

- **LCD Control Circuit**
- **LCD Common Driver**
- **LCD Segment Driver**
- **LCD Waveform**

For a more detailed description of how the LCD operates and its basic construction, refer to Appendix C of this manual.

LCD Control Circuit

The LCD Control Circuit of the Tandy 200 consists of the LCDC (HD61830B) and 8K-byte RAM.

The LCDC generates driving signals for LCD by receiving the instructions and data from the CPU. The driving signals for LCD are divided into two groups: one is the timing signal for the segment driver and common driver, another is the data to display.

The CLKL signal, divided 2.4576 MHz clock signal by two at M34, is supplied to the RC terminal of the LCDC.

One bit value of the 8K-byte RAM connected to LCDC corresponds to one dot of illumination or non-illumination on the LCD screen. These data are converted into the serial data D1 and D2 at the LCDC, and then sent to the segment driver.

Figure 32 shows the internal block diagram of HD61830B.

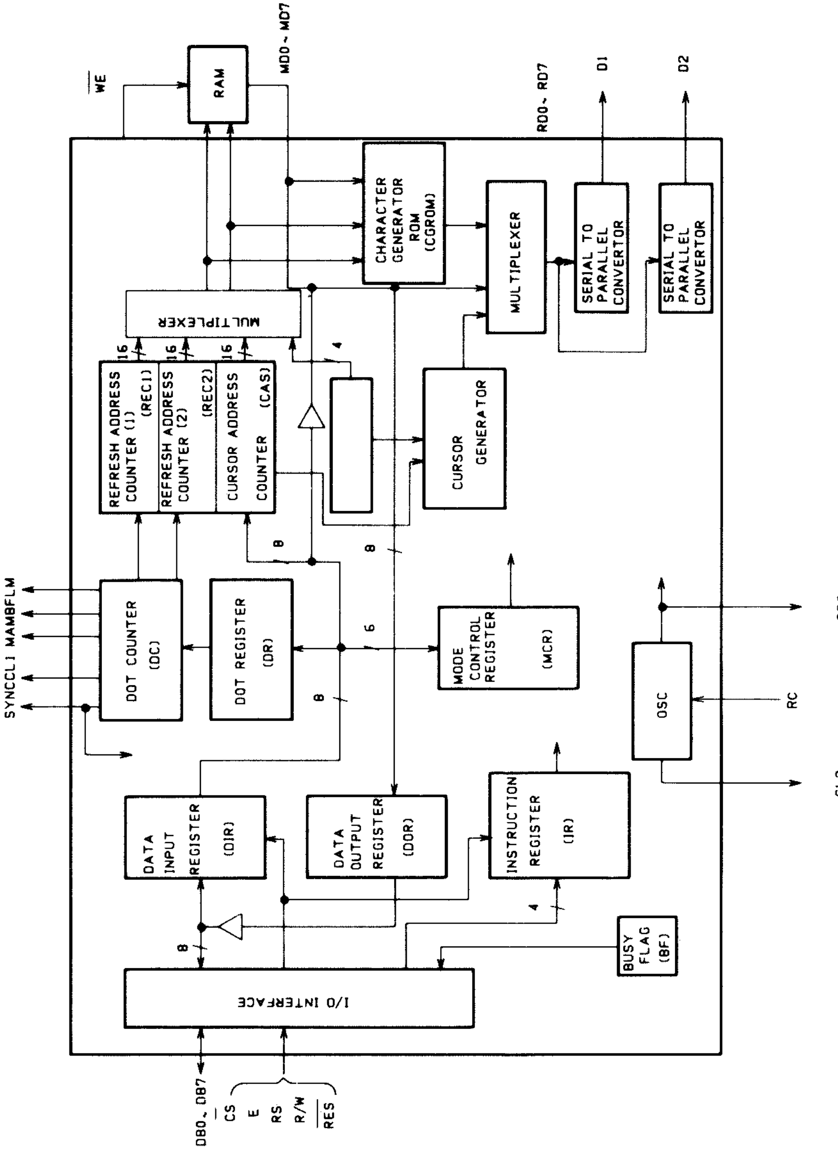


Figure 32. Internal Block Diagram of HD61830B

The Common Driver (HD61103)

The Tandy 200 uses two common driver ICs: M507 and M508. M507 controls the upper half of the LCD screen and M508 controls the lower half of the LCD screen.

The FRM signal defines the periodic frequency of one-screen display, and determines 80 Hz for the Tandy 200.

The MB signal is used for changing the driver signal to AC, because the continuous application of DC to the LCD would shorten the LCD element life.

The CL1 signal is used for the shift clock of the internal shift register.

Figures 33 and 34 show the internal block diagram of HD61103 and output waveform of HD61103.

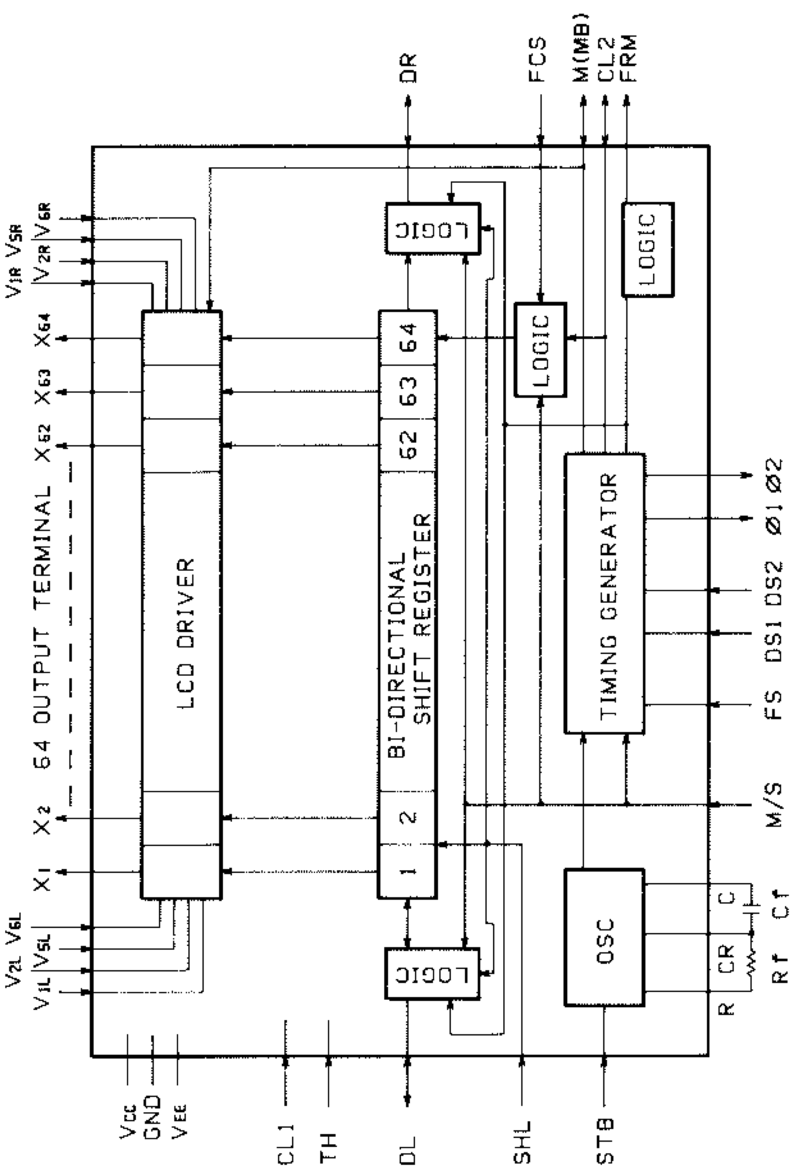


Figure 33. Internal Block Diagram of HD61103

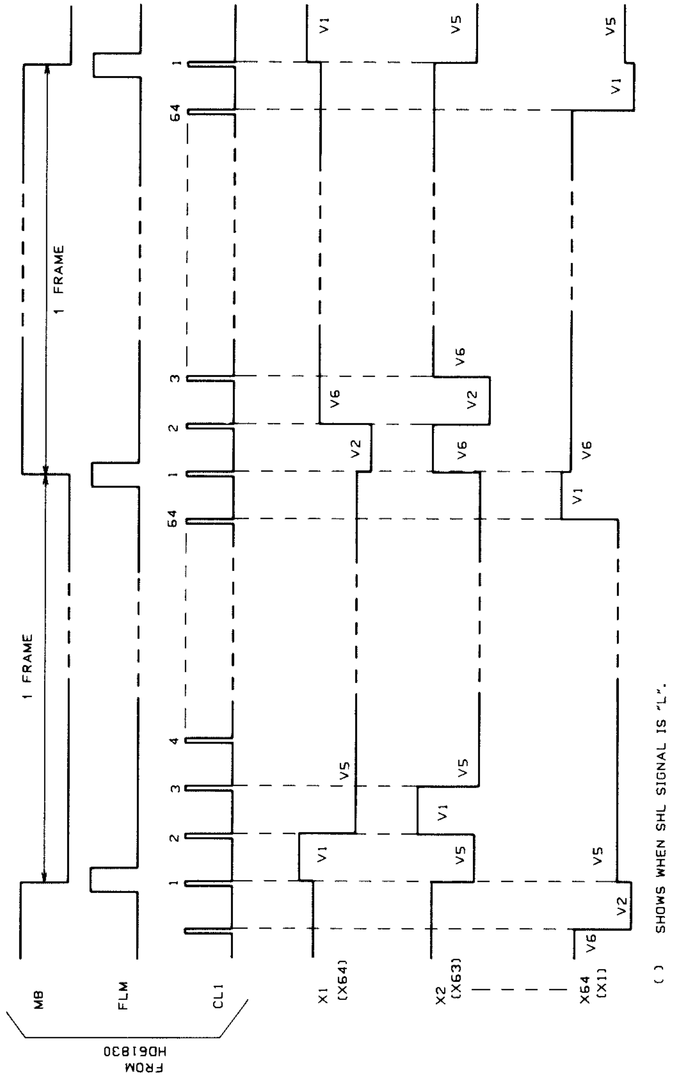


Figure 34. Output Waveform of HD61103

Segment Driver (HD61100)

The Tandy 200 uses six segment driver ICs (HD61100), and each IC has 80 output drivers.

HD61100 is a driver IC for the LCD display. It receives and latches the serial display data from the LCDC, and generates the segment driver signals.

The CL1, CL2, D1, D2 and MB signals are supplied from the LCDC. The CL1 signal is used for the latch clock of the internal 80 latches. Synchronizing with the fall of CL1, the segment driver signals corresponding to the display data are output.

The CL2 signal is used for the shift clock of the display data. The MB signal changes output signals to AC.

The D1 signal is the data to display on the upper half of the LCD screen and the D2 signal is the data to display on the lower half of the LCD screen.

Figures 35 and 36 show the internal block diagram of HD61100 and output waveform of HD61100.

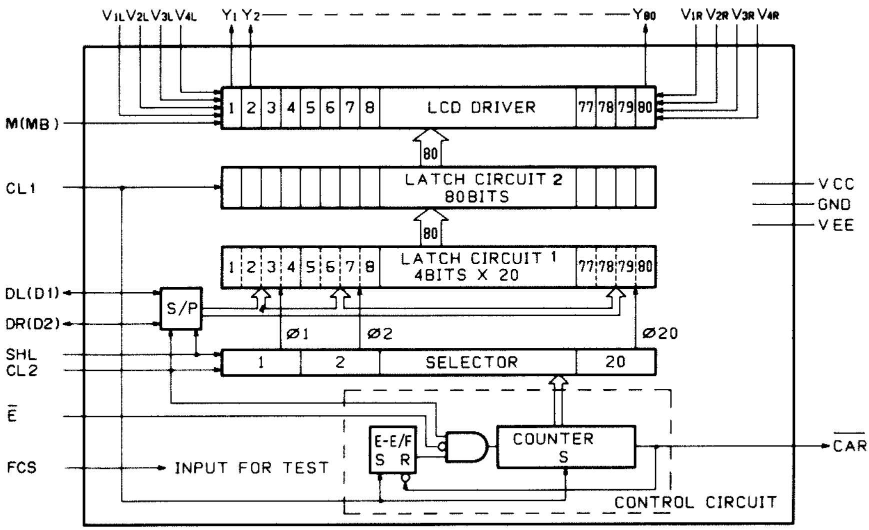


Figure 35. Internal Block Diagram of HD61100

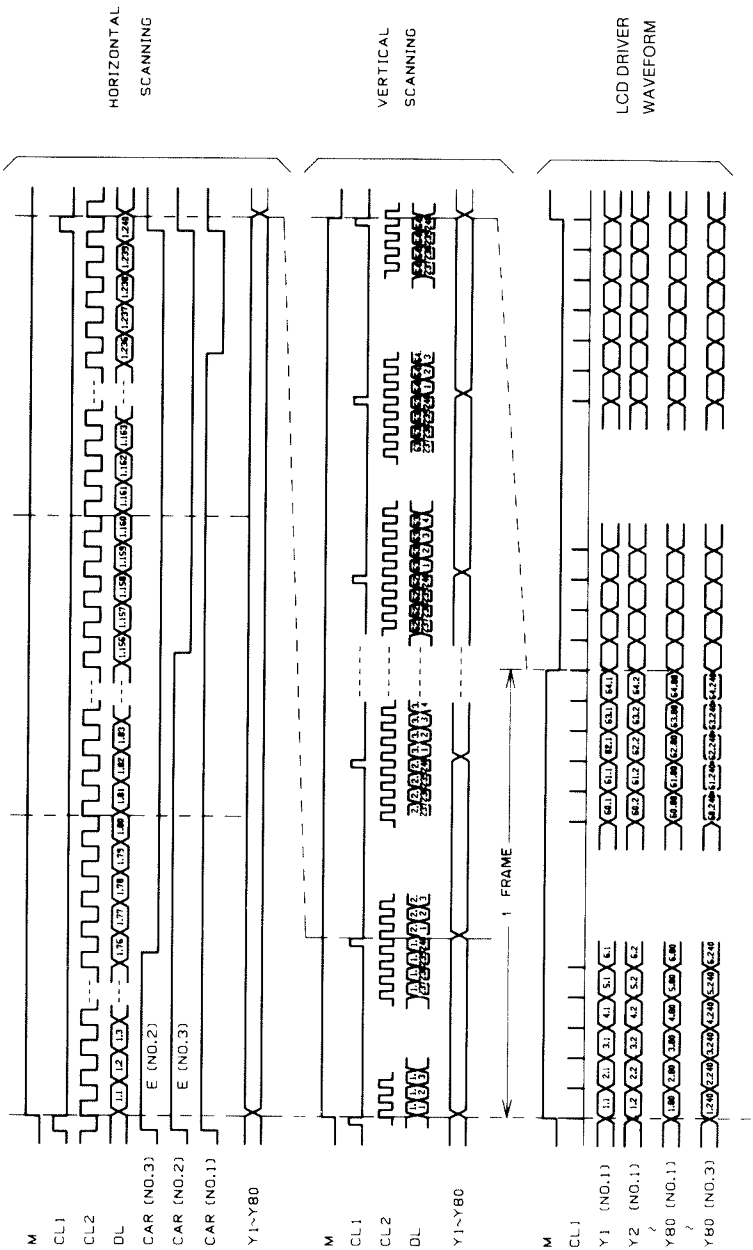


Figure 36. Output Waveform of HD61100

LCD Waveform

In order to drive the liquid-crystal elements by the 1/64 duty line-sequential drive method, the LCD of the Tandy 200 makes sequential selection of the 64 scanning electrodes.

For each dot, the display signal passes through the signal electrodes and is applied 64 times for one display.

At this point, the signal is necessary at each dot only one time, and the signal for the other 63 times corresponds to other dots on the same signal electrode.

The maximum voltage applied to the common electrode and segment electrode is the potential difference between V1 and V2.

In addition, "a" is the bias coefficient which determines from the standpoint of contrast, the maximum ratio between the illumination voltage and the non-illumination voltage.

When that ratio is greatest in relation to the effective ON and OFF voltages, "a" = 9.0.

Thus, for V1, V2, V3, V4, V5 and V6:

V1 = VDD(+5V)
V2 = V0(approximately −7V to −10V)
V3 = VDD −2V/a
V4 = VDD −(1−2/a)V
V5 = VDD −(1−1/a)V
V6 = VDD −V/a

Note: Absolute value of "V" equal absolute value of "VDD" plus absolute value of "V0".

Figure 37 shows the driving waveform for illumination and non-illumination.

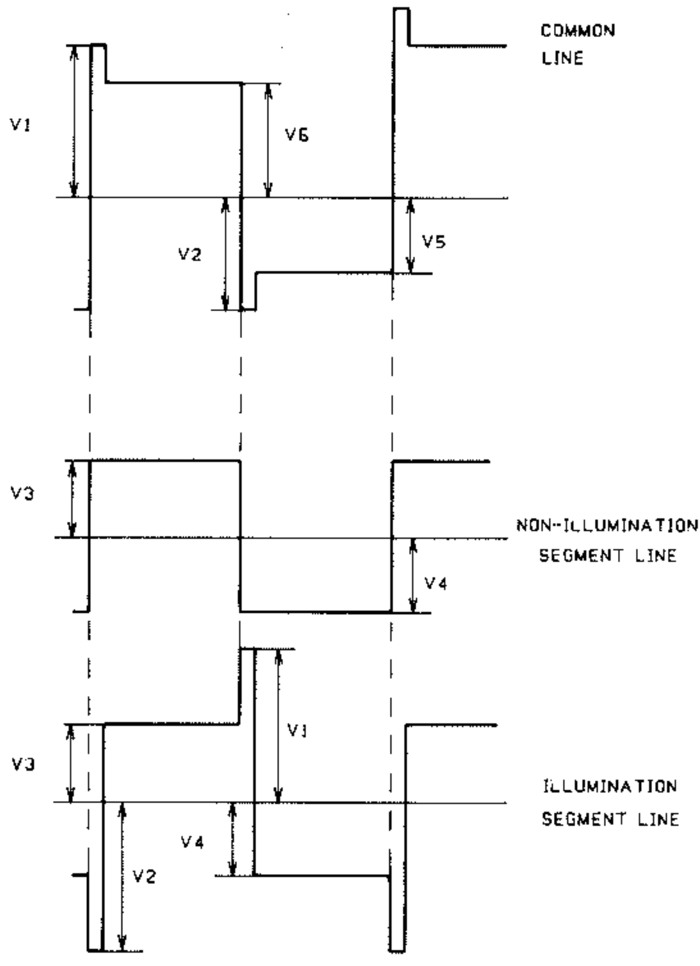


Figure 37. Driving Waveform of LCD

Power Supply and Auto-Power ON/OFF Circuit

The power supply circuit develops the following voltages:

- VDD (+5 volts DC)
- VEE (−5 volts DC)
- VLCD (−10 volts DC)
- VB
- VIN
- VD
- VR
- VNICD

VDD is supplied to all of the ICs except the main memory, TIMER (RP5C01), M24, M25 and M26.

VEE is used as a negative power source for the operational amplifiers.

VLCD is supplied to the LCD PCB through T27 for the LCD driving voltage.

VB is supplied to the main memory, TIMER, M24, M25 and M26.

VR is used for the input voltage to the DC/DC converter circuit. When the internal circuit is modified for use of Nickel-Cadmium batteries, VIN is supplied to the four Nickel-Cadmium batteries installed into the battery compartment.

This power source charges the Nickel-Cadmium batteries whenever an AC adapter is connected to the Tandy 200.

Power Distribution

Figure 38 shows the power distribution of the Tandy 200. In this circuit, R165 is used as the current limiter during the charge. D11 protects the power supply from the reverse current. The power control circuit controls the DC/DC converter circuit corresponding with the POWER, $\overline{\text{ALM}}$, PCS and BELL signals.

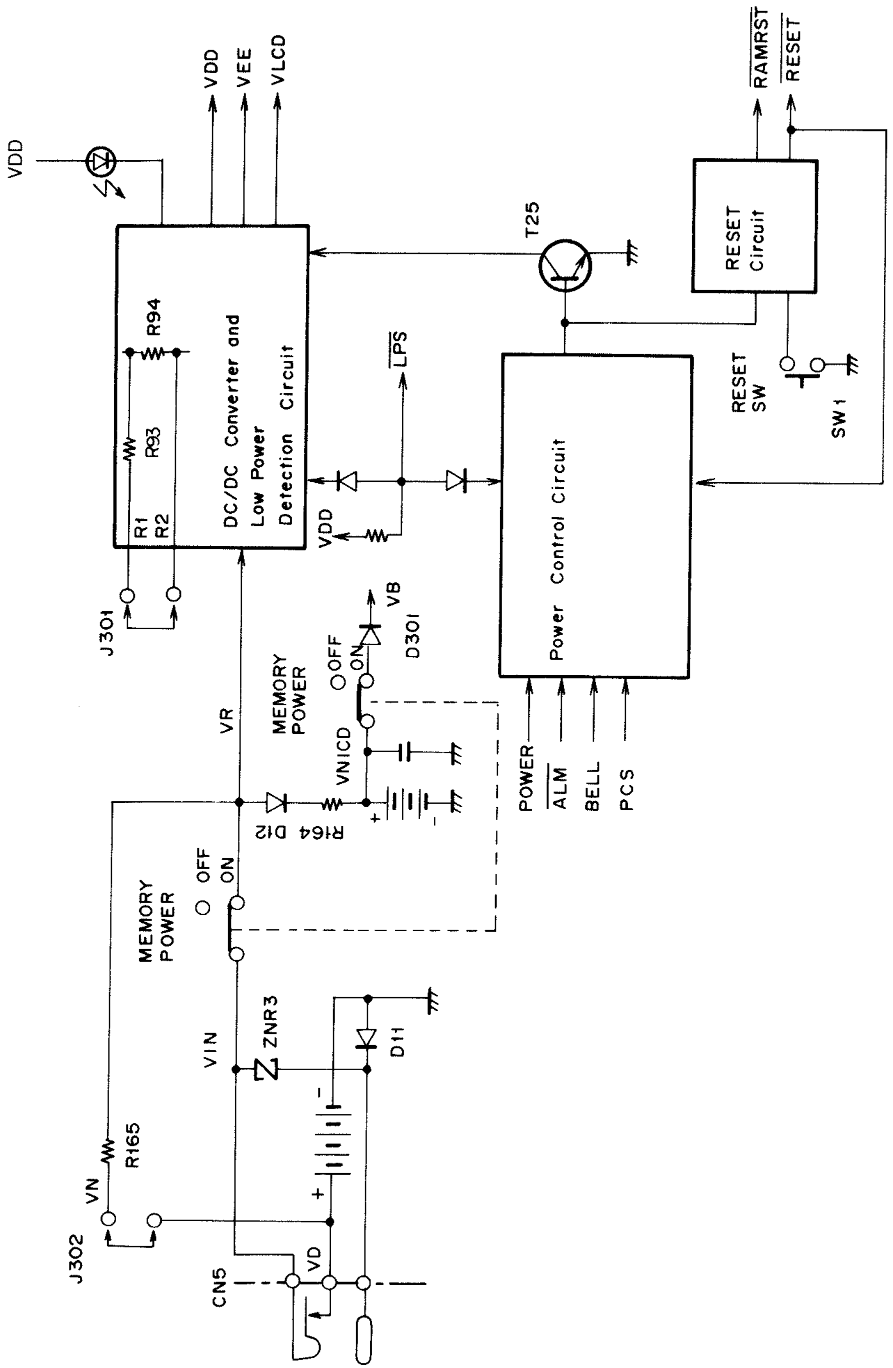


Figure 38. Power Distribution

DC/DC Converter

OT2 is a converter transformer which oscillates T20 and T21 and generates voltages at the secondary side of the transformer. At the same time the power is switched ON, a very slight collector current flows to T20 and T21. Also, voltage between pin 3 and pin 6 of the converter transformer is generated, and the T21 base potential becomes positive. In other words, the base polarity becomes biased in the forward direction. This voltage causes the T20 and T21 base current to flow, and the collector current is increased. When the current can no longer increase, because of transistor saturation and converter coil resistance, the voltage between pins 3 and 6 begins to attenuate, causing T20 and T21 to be cut off all at once because of the reverse playback action. Until immediately before the transistor is cut off, excitation current flows to the transformer. Because the current is suddenly dropped as a result of the transistor cut-off, a counter voltage is generated, the distributed capacity of the coil is changed, and, as a result, an oscillation voltage is generated at the base coil. Then, when the base potential progresses to a half cycle of the oscillation voltage, it is biased in the forward direction, T20 and T21 are switched ON once again. In this way, AC voltage corresponding to the number of windings is generated at the secondary side of the converter, and this voltage is rectified and smoothed by D13, D14, D15, C62, C63 and C64.

Low Power Detection Circuit

The low-power detection circuit illuminates an LED warning lamp when the battery voltage decreases. If it continues decreasing, the system power will be switched OFF just before the voltage becomes so low that the converter cannot operate.

There are about 20 minutes between the time when the LED lamp illuminates and the system is switched OFF.

Battery voltage is detected by splitting the resistance of R91, R92, R94 and R95. When battery voltage (VR) becomes 4.2V $\pm$0.1V, T18 is switched OFF. T19 is switched ON, T23 is driven, and the LED illuminates. (The LED is located on the keyboard PCB.)

In addition, the value of the detected voltage is changed by R93 because of a difference between the output voltage of Alkaline-manganese and Nickel-Cadmium batteries.

The R1 and R2 signals are shorted on the memory PCB when the internal circuit is modified for use of Nickel-Cadmium batteries.

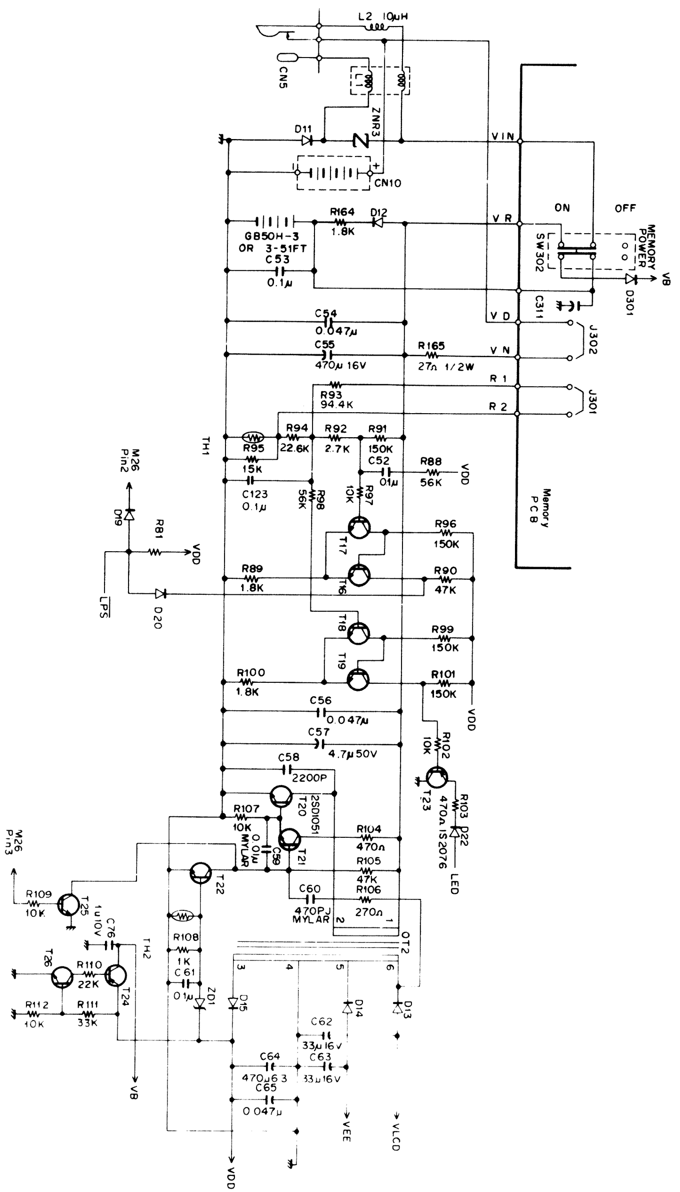


Figure 39. DC/DC Converter and Low Power Detection Circuit

Power Control Circuit

This circuit controls the oscillation of the DC/DC converter circuit by using T25. There are four methods to control the power ON/OFF. In this circuit, the VDD terminals of M24, M25 and M26 are connected to VB, since these ICs must operate in power-off condition.

1. Power-up using the POWER switch

If a customer presses the POWER switch on the keyboard during power-off condition, the following events occur:

a. A positive short pulse is sent to the base of T32 through C70, then T32 is switched on.

b. On the other hand, the Bell and $\overline{\text{RESET}}$ signals are "L" during power-off condition, but the input pin 8 of the gate M24 is pulled up to VB. Thus the output pin 10 of the gate M24 becomes "L," which enables the gate M25.

c. T31 is switched on. This "H" level signal is supplied to the RESET terminal of the flip-flop M26 and then the flip-flop M26 is reset.

d. The output pin 13 of the flip-flop M26 becomes "L" and T25 is switched off.

e. The DC/DC converter circuit starts the oscillation, if the proper DC level of VR is supplied to this circuit.

f. VDD reaches the specified DC level, T16 is switched off. At the same time, the $\overline{\text{LPS}}$ signal becomes "H" and is sent to the TRAP terminal of the CPU after inverted at M35.

g. When VDD reaches a constant DC level to operate the CPU, T28 is switched on and T29 is switched off. The $\overline{\text{RESET}}$ signal becomes "H," then the CPU begins the "Warm-Start" process. After completion of the "Warm-Start," the CPU drops the BELL signal.

h. The output pin 10 of the gate M24 becomes "H" and the output pin 10 of the gate M25 becomes "L," then the Tandy 200 will be able to operate.

2. Power-down using the POWER switch

If a customer presses the POWER switch on the keyboard during power-on condition, the following events occur:

a. A positive short pulse is sent to the base of the T32 through C70, and then T32 is switched on.

b. On the other hand, the cross-couple consisting of the gate M24 was set by the BELL signal in the last power-on sequence. Thus the output pin 11 of the gate M25 becomes "H."

c. The flip-flop M26 is clocked by this "H" level signal. The output pin 2 of flip-flop M26 becomes "L."

d. The LPS signal goes "L" and is sent to the TRAP terminal of the CPU after being inverted at M35.

e. This signal notifies the CPU when the customer presses the POWER switch. The CPU starts the internal power-down process. After completion of this process, the CPU sends the PCS signal passing through the PB of the 81C55.

f. Receiving the PCS signal, the output pin 4 of the gate M24 becomes "L."

g. The flip-flop M26 is set. The output pin 13 of M26 becomes "H" and T25 is switched on.

h. This causes the DC/DC converter to stop the oscillation. Then the Tandy 200 will not be able to operate.

3. Power-up using the $\overline{\text{ALM}}$ signal

The $\overline{\text{ALM}}$ signal becomes "L" when the time matches the value set by the POWER command in BASIC. The $\overline{\text{ALM}}$ signal is generated by the TIMER IC on the memory PCB. T31 is switched on by the "L" level $\overline{\text{ALM}}$ signal.

The remaining sequence follows the power-up using the POWER switch.

4. Power-down using the PCS signal

To control the power supply, the CPU sends the PCS signal if the automatic Power-Off limit reaches the value corresponding with the 1st parameter of the POWER command in BASIC.

The remaining sequence follows the Power-Down using the POWER switch.

Reset Circuit

This circuit supplies the CPU $\overline{\text{RESET}}$ signal and also the RAMRST signal as the RAM protecting signal when the power decreases. R113 and C66 delay the introduction of input power so that T28 is switched on and T29 is switched off after VDD is activated, with the result that the $\overline{\text{RESET}}$ signal changed from "L" to "H." In the same way, the RAMRST signal is generated by T30 and changes from "H" to "L." Thermistor TH3 suppresses the $\overline{\text{RESET}}$ signal fluctuations due to temperature. T27 receives the signal during automatic power OFF, short-circuiting both end of C66, and resets the system. The $\overline{\text{RESET}}$ signal is active "L" and the RAMRST signal is active "H."

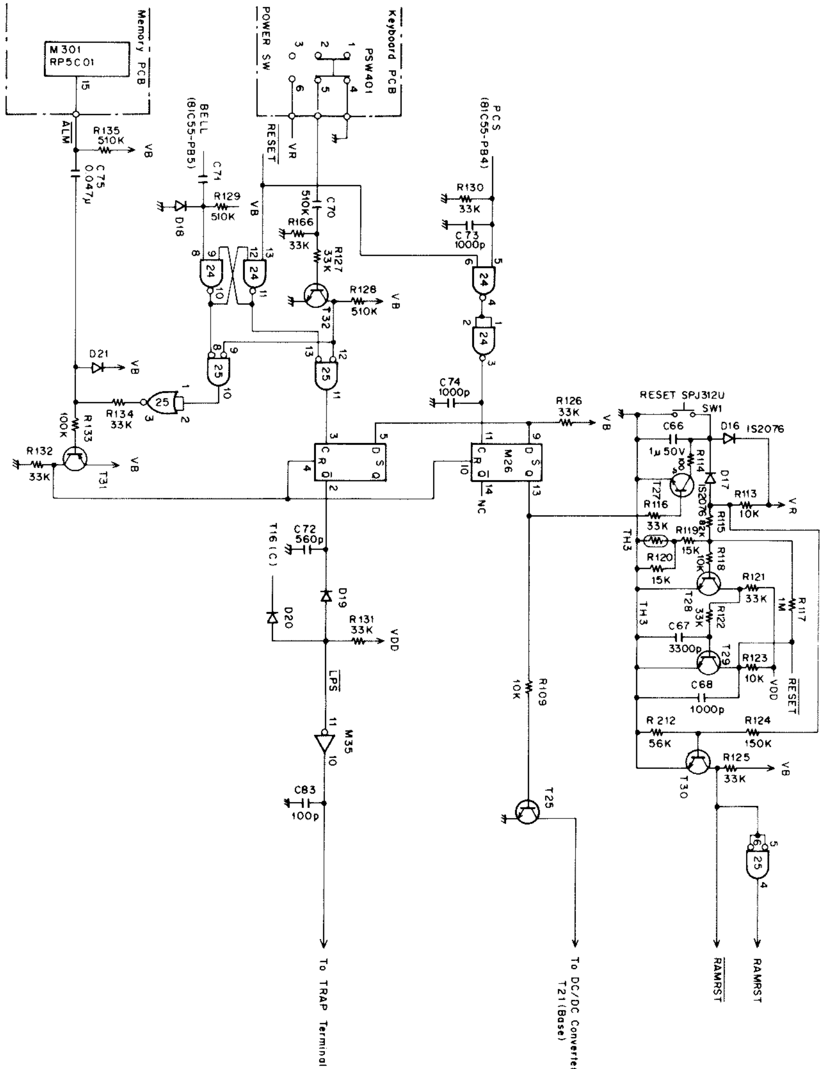


Figure 40. Power Control and Reset Circuit

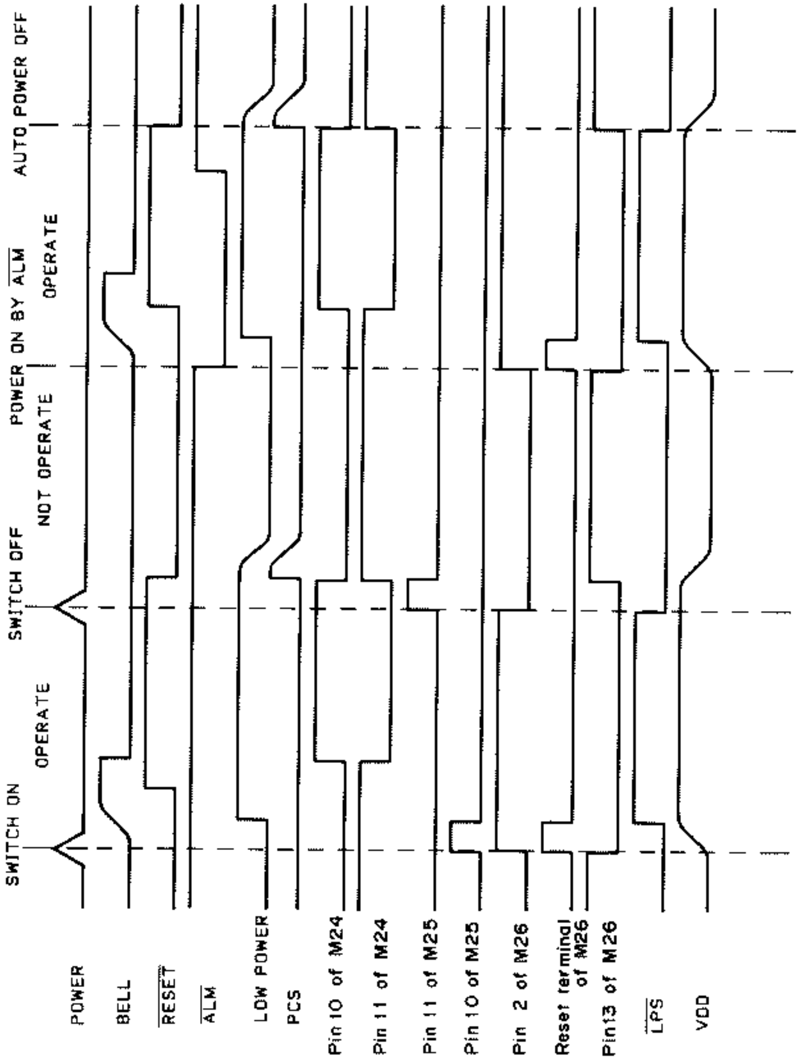


Figure 41. Power-Up/Down Sequence

APPENDIX A/INSTALLATIONS

Installation of Optional RAMs and ROM

- Using the coin, remove the optional RAM and ROM cover on the bottom case.
- Insert the optional RAMs into the IC sockets marked M306 and M307. In this case, the IC socket M307 is used for the RAM #1 and M306 is RAM #2.
- Insert the optional ROM into the IC socket marked M308.

Installation of Nickel-Cadmium Batteries

- Remove the memory PCB (Refer to Section II, Disassembly Instruction).
- Install the modification jumpers into the through holes marked J301 and J302.
- Re-assemble the unit.

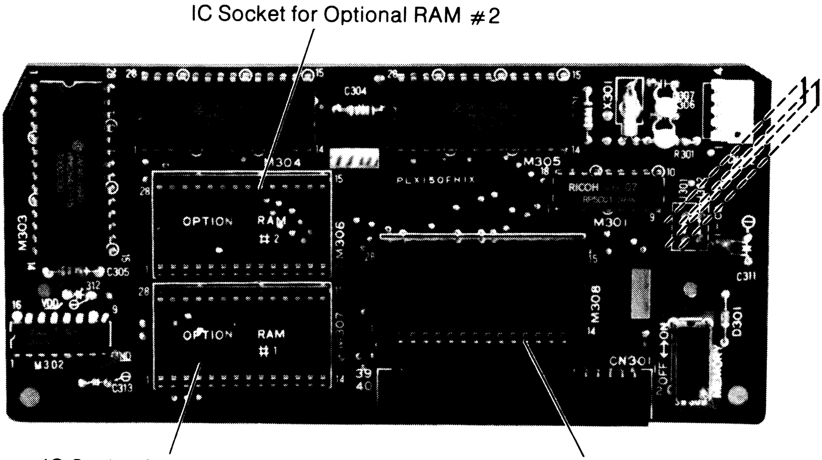


Figure A-1. Memory PCB

- Remove the battery cover and install the four Nickel-Cadmium batteries into the battery compartment.
- Drill the screw hole on the battery cover using the tapping screw Ⓐ and secure the battery cover and bottom case.
- Stick the red label Ⓑ on the battery cover.

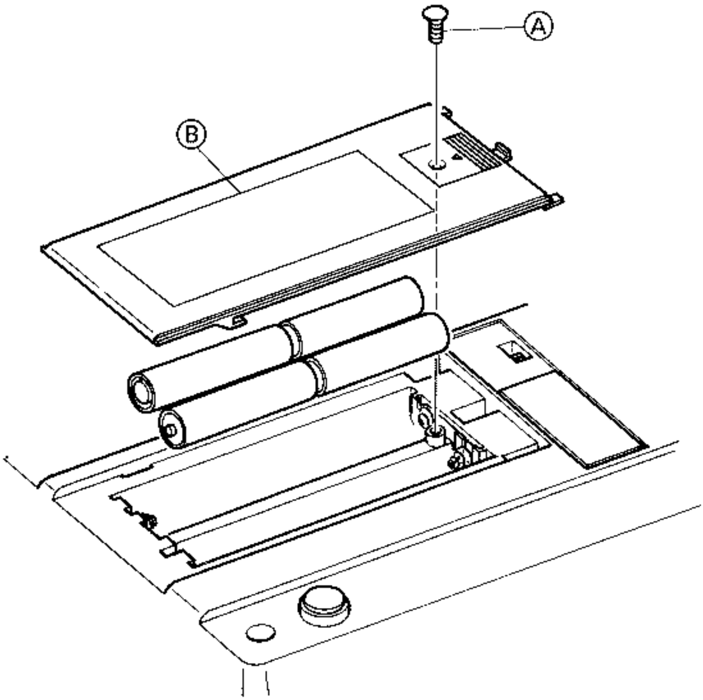


Figure A-2. Installation of Nickel-Cadmium Batteries

APPENDIX B/KEYBOARD LAYOUT, CONNECTOR PIN ASSIGNMENTS AND CHARACTER CODE TABLE

Keyboard Layout

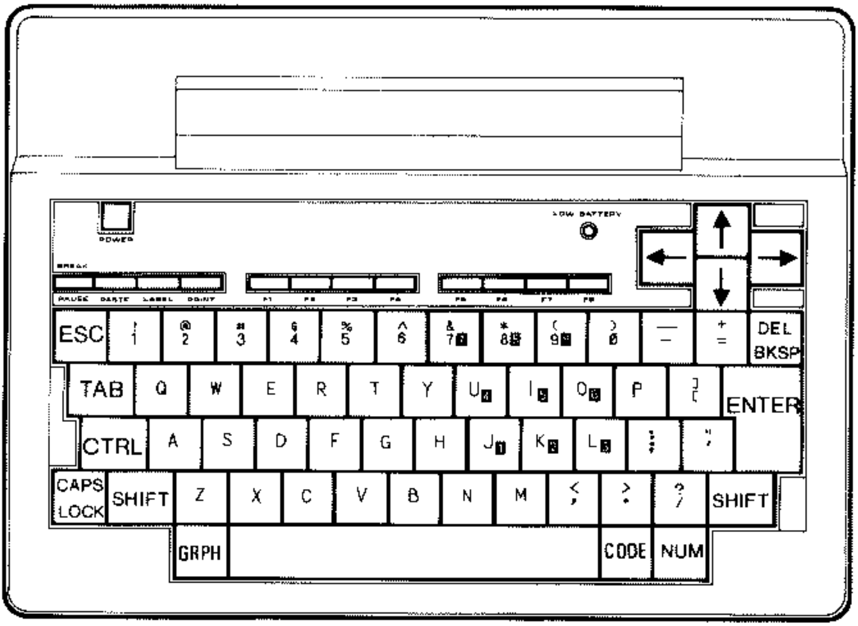


Figure B-1. Keyboard Layout

Connector Pin Assignments

System Bus Interface

Pin No.	Symbol	Description
1	VDD	
2	VDD	
3	GND	
4	GND	
5	D0	Address and data signal bit 0
6	D1	Address and data signal bit 1
7	D2	Address and data signal bit 2
8	D3	Address and data signal bit 3
9	D4	Address and data signal bit 4
10	D5	Address and data signal bit 5
11	D6	Address and data signal bit 6
12	D7	Address and data signal bit 7
13	A8	Address signal bit 8
14	A9	Address signal bit 9
15	A10	Address signal bit 10
16	A11	Address signal bit 11
17	A12	Address signal bit 12
18	A13	Address signal bit 13
19	A14	Address signal bit 14
20	A15	Address signal bit 15
21	GND	
22	GND	
23	$\overline{\text{RD}}$	Read enable signal
24	$\overline{\text{WR}}$	Write enable signal
25	IO/$\overline{\text{M}}$	I/O or memory select signal
26	S0	Status 0 signal
27	ALE	Address latch enable signal
28	S1	Status 1 signal
29	CLK	CLock signal
30	$\overline{\text{IOCONT}}$	I/O controller select signal
31	E	I/O or memory access enable signal
32	RESET	Reset signal
33	INTR	Interrupt request signal
34	$\overline{\text{INTA}}$	Interrupt acknowledge signal
35	GND	
36	GND	
37	$\overline{\text{RAMRST}}$	RAM enable signal
38	NC	
39	NC	
40	NC	

Table B-1. System Bus Connector Pin Assignments

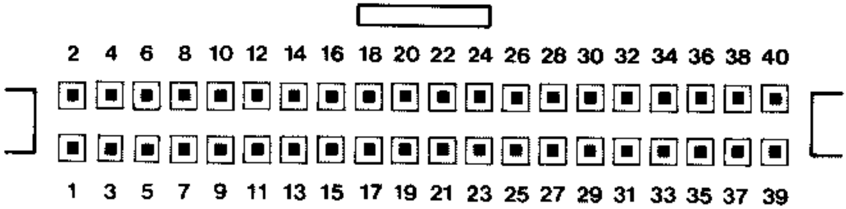


Figure B-2. System Bus Connector

RS-232C Interface

Pin No.	Symbol	Description
1	GND	
2	TXR	Transmit Data
3	RXR	Receive Data
4	RTS	Request to send
5	CTS	Clear to send
6	DSR	Data set ready
7	GND	
8	CD	Carrier detect
9	NC	
10	NC	
11	NC	
12	NC	
13	NC	
14	NC	
15	NC	
16	NC	
17	NC	
18	NC	
19	NC	
20	DTR	Data terminal ready
21	NC	
22	NC	
23	NC	
24	NC	
25	NC	

Table B-2. RS-232C Connector Pin Assignments

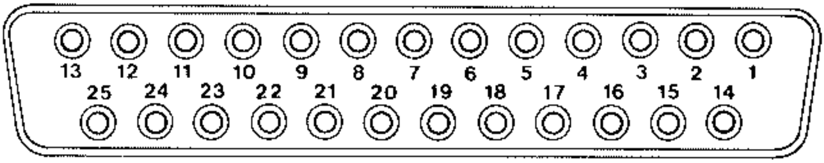


Figure B-3. RS-232C Connector

Printer Interface

Pin No.	Symbol	Description
1	**$\overline{\text{STROBE}}$**	STROBE Pulse
2	**GND**	
3	**PD0**	Bit 0 of Print Data
4	**GND**	
5	**PD1**	Bit 1 of Print Data
6	**GND**	
7	**PD2**	Bit 2 of Print Data
8	**GND**	
9	**PD3**	Bit 3 of Print Data
10	**GND**	
11	**PD4**	Bit 4 of Print Data
12	**GND**	
13	**PD5**	Bit 5 of Print Data
14	**GND**	
15	**PD6**	Bit 6 of Print Data
16	**GND**	
17	**PD7**	Bit 7 of Print Data
18	**GND**	
19	**NC**	
20	**GND**	
21	**BUSY**	Busy signal for Computer
22	**GND**	
23	**NC**	
24	**GND**	
25	**$\overline{\text{BUSY}}$**	Select signal
26	**NC**	

Table B-3. Printer Connector Pin Assignments

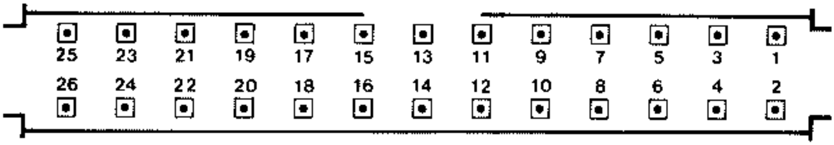


Figure B-4. Printer Connector

Cassette Interface

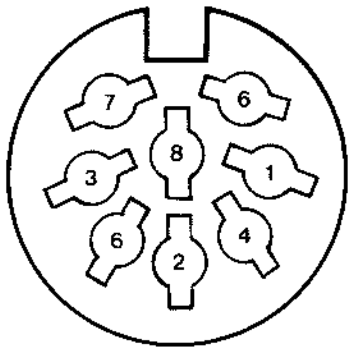


Figure B-5. Cassette Connector

MODEM Interface

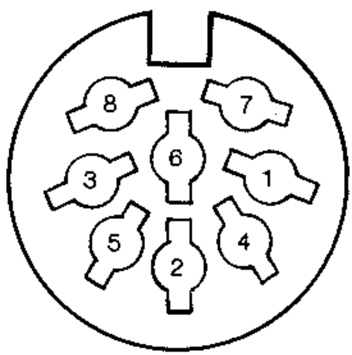


Figure B-6. MODEM Connector

Bar Code Reader Interface

Pin No.	Symbol	Description
1	NC	
2	R × DB	Receive data from bar code reader
3	NC	
4	NC	
5	NC	
6	NC	
7	GND	
8	NC	
9	VDD	

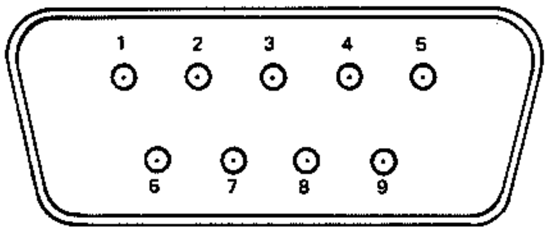


Figure B-7. Bar Code Reader Connector

Character Code Table

Decimal	Hex	Binary	Displayed Character	Keyboard Character
00	00	00000000		CTRL @
1	01	00000001		CTRL A
2	02	00000010		CTRL B
3	03	00000011		CTRL C
4	04	00000100		CTRL D
5	05	00000101		CTRL E
6	06	00000110		CTRL F
7	07	00000111		CTRL G
8	08	00001000		CTRL H
9	09	00001001		CTRL I
10	0A	00001010		CTRL J
11	0B	00001011		CTRL K
12	0C	00001100		CTRL L
13	0D	00001101		CTRL M
14	0E	00001110		CTRL N
15	0F	00001111		CTRL O
16	10	00010000		CTRL P
17	11	00010001		CTRL Q
18	12	00010010		CTRL R
19	13	00010011		CTRL S
20	14	00010100		CTRL T
21	15	00010101		CTRL U
22	16	00010110		CTRL V
23	17	00010111		CTRL W
24	18	00011000		CTRL X
25	19	00011001		CTRL Y
26	1A	00011010		CTRL Z
27	1B	00011011		ESC
28	1C	00011100		→
29	1D	00011101		←
30	1E	00011110		↑
31	1F	00011111		↓
32	20	00100000		SPACEBAR
33	21	00100001	!	!
34	22	00100010	"	"
35	23	00100011	#	#
36	24	00100100	$	$
37	25	00100101	%	%
38	26	00100110	&	&
39	27	00100111	'	'
40	28	00101000	(	(
41	29	00101001	)	)
42	2A	00101010	*	*
43	2B	00101011	+	+
44	2C	00101100	,	,
45	2D	00101101	-	-
46	2E	00101110	.	.
47	2F	00101111	/	/
48	30	00110000	Ø	0
49	31	00110001	1	1

Decimal	Hex	Binary	Displayed Character	Keyboard Character
50	32	00110010	2	2
51	33	00110011	3	3
52	34	00110100	4	4
53	35	00110101	5	5
54	36	00110110	6	6
55	37	00110111	7	7
56	38	00111000	8	8
57	39	00111001	9	9
58	3A	00111010	:	:
59	3B	00111011	;	;
60	3C	00111100	<	<
61	3D	00111101	=	=
62	3E	00111110	>	>
63	3F	00111111	?	?
64	40	01000000	@	@
65	41	01000001	A	A
66	42	01000010	B	B
67	43	01000011	C	C
68	44	01000100	D	D
69	45	01000101	E	E
70	46	01000110	F	F
71	47	01000111	G	G
72	48	01001000	H	H
73	49	01001001	I	I
74	4A	01001010	J	J

Decimal	Hex	Binary	Display Character	Keyboard Character
75	4B	01001011	K	K
76	4C	01001100	L	L
77	4D	01001101	M	M
78	4E	01001110	N	N
79	4F	01001111	O	O
80	50	01010000	P	P
81	51	01010001	Q	Q
82	52	01010010	R	R
83	53	01010011	S	S
84	54	01010100	T	T
85	55	01010101	U	U
86	56	01010110	V	V
87	57	01010111	W	W
88	58	01011000	X	X
89	59	01011001	Y	Y
90	5A	01011010	Z	Z
91	5B	01011011	[	[
92	5C	01011100	\	-
93	5D	01011101	]	|
94	5E	01011110	^	-
95	5F	01011111	_	_
96	60	01100000	`	[
97	61	01100001	a	a
98	62	01100010	b	b
99	63	01100011	c	c

Decimal	Hex	Binary	Displayed Character	Keyboard Character
100	64	01100100	d	d
101	65	01100101	e	e
102	66	01100110	f	f
103	67	01100111	g	g
104	68	01101000	h	h
105	69	01101001	i	i
106	6A	01101010	j	j
107	6B	01101011	k	k
108	6C	01101100	l	l
109	6D	01101101	m	m
110	6E	01101110	n	n
111	6F	01101111	o	o
112	70	01110000	p	p
113	71	01110001	q	q
114	72	01110010	r	r
115	73	01110011	s	s
116	74	01110100	t	t
117	75	01110101	u	u
118	76	01110110	v	v
119	77	01110111	w	w
120	78	01111000	x	x
121	79	01111001	y	y
122	7A	01111010	z	z
123	7B	01111011	{	9
124	7C	01111100	¦	_
125	7D	01111101	}	0
126	7E	01111110	~	}
127	7F	01111111		
128	80	10000000		p
129	81	10000001		m
130	82	10000010		f
131	83	10000011		x
132	84	10000100		c
133	85	10000101		a
134	86	10000110		h
135	87	10000111		t
136	88	10001000	π	1
137	89	10001001	√	r
138	8A	10001010	≠	/
139	8B	10001011	Σ	s
140	8C	10001100	≈	
141	8D	10001101	±	=
142	8E	10001110	∫	i
143	8F	10001111		e
144	90	10010000		y
145	91	10010001		u
146	92	10010010	↕	:
147	93	10010011		q
148	94	10010100		w
149	95	10010101	↗	b

Decimal	Hex	Binary	Displayed Character	Keyboard Character
150	96	10010110	‡	n
151	97	10010111	✂	.
152	98	10011000	↑	o
153	99	10011001	↓	,
154	9A	10011010	→	l
155	9B	10011011	←	k
156	9C	10011100	♣	2
157	9D	10011101	◇	3
158	9E	10011110	♡	4
159	9F	10011111	♤	5
160	A0	10100000	´	´
161	A1	10100001	à	z
162	A2	10100010	c	f
163	A3	10100011	£	8
164	A4	10100100	`	"
165	A5	10100101	µ	]
166	A6	10100110	◆	)
167	A7	10100111	▼	_
168	A8	10101000	†	+
169	A9	10101001	§	s
170	AA	10101010	▣	R
171	AB	10101011	▣	Y
172	AC	10101100	¼	p
173	AD	10101101	¾	;
174	AE	10101110	½	/
175	AF	10101111	¶	0
176	B0	10110000	¥	7
177	B1	10110001	Ă	Q
178	B2	10110010	Ŏ	O
179	B3	10110011	Ŭ	U
180	B4	10110100	¢	6
181	B5	10110101	~	[
182	B6	10110110	ä	q
183	B7	10110111	ö	o
184	B8	10111000	ü	u
185	B9	10111001	ß	S
186	BA	10111010	™	T
187	BB	10111011	é	d
188	BC	10111100	ù	m
189	BD	10111101	è	c
190	BE	10111110	¨	=
191	BF	10111111	ƒ	F
192	C0	11000000	â	1
193	C1	11000001	ê	3
194	C2	11000010	î	B
195	C3	11000011	ô	9
196	C4	11000100	û	7
197	C5	11000101	^	–
198	C6	11000110	ë	e
199	C7	11000111	ï	i

Decimal	Hex	Binary	Displayed Character	Keyboard Character
200	C8	11001000	á	a
201	C9	11001001	í	k
202	CA	11001010	ó	l
203	CB	11001011	ú	i
204	CC	11001100	j	!
205	CD	11001101	Ñ	n
206	CE	11001110	Š	v
207	CF	11001111	Ő	b
208	D0	11010000	Ä	X
209	D1	11010001	æ	x
210	D2	11010010	Á	W
211	D3	11010011	à	w
212	D4	11010100	Ø	>
213	D5	11010101	ø	.
214	D6	11010110	Ñ	N
215	D7	11010111	É	D
216	D8	11011000	Á	A
217	D9	11011001	f	K
218	DA	11011010	Ó	L
219	DB	11011011	Ú	J
220	DC	11011100	¿	?
221	DD	11011101	Ù	M
222	DE	11011110	È	C
223	DF	11011111	À	Z
224	E0	11100000		Z

Decimal	Hex	Binary	Displayed Character	Keyboard Character
225	E1	11100001	▘	!
226	E2	11100010	▝	@
227	E3	11100011	▖	#
228	E4	11100100	▗	$
229	E5	11100101	▚	%
230	E6	11100110	▞	-
231	E7	11100111	▀	Q
232	E8	11101000	▄	W
233	E9	11101001	▌	E
234	EA	11101010	▐	R
235	EB	11101011	▛	A
236	EC	11101100	▜	S
237	ED	11101101	▙	D
238	EE	11101110	▟	F
239	EF	11101111	█	X
240	F0	11110000	┌	U
241	F1	11110001	─	P
242	F2	11110010	┐	O
243	F3	11110011	┬	I
244	F4	11110100	├	J
245	F5	11110101	│	:
246	F6	11110110	└	M
247	F7	11110111	┘	>
248	F8	11111000	┴	<
249	F9	11111001	┤	L

Decimal	Hex	Binary	Displayed Character	Keyboard Character
250	FA	11111010	┼	K
251	FB	11111011	◤	H
252	FC	11111100	◢	T
253	FD	11111101	◥	G
254	FE	11111110	◣	Y
255	FF	11111111	▒	C

APPENDIX C/TECHNICAL INFORMATION

80C85A

General Description

The 80C85A is a complete 8-bit parallel central processor implemented in silicon gate C-MOS technology and compatible with 8085A.

It is designed with same processing speed and lower power consumption compared with 8085A, thereby offering a high level of system integration.

The 80C85A uses a multiplexed address/data bus. The address is split between the 8-bit address bus and the 8-bit data bus.

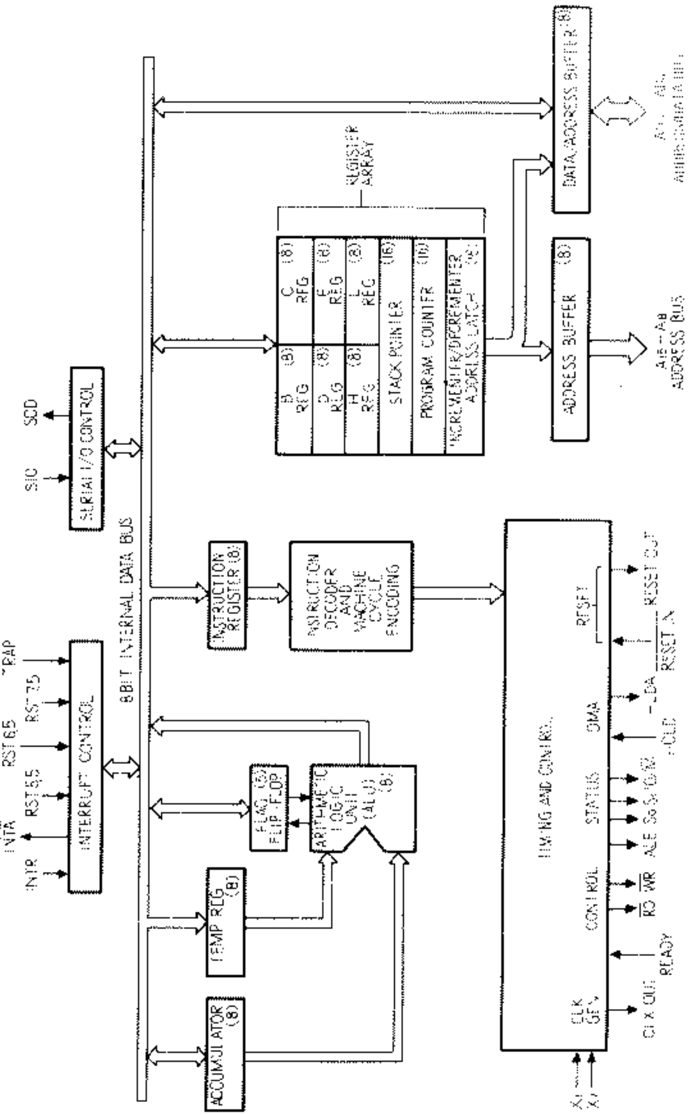


Figure C-1. Functional Block Diagram

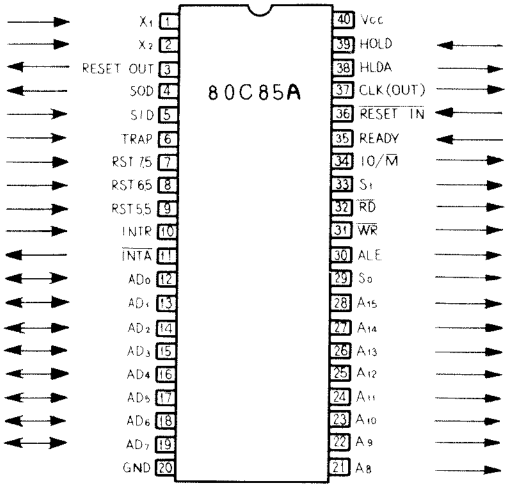


Figure C-2. Pin Configuration of 80C85A

Functional Pin Description

A_8 – A_{15} (Output, 3-state)
Address Bus: The most significant 8 bits of the memory address or the 8 bits of the I/O address, 3-stated during Hold and Halt modes and during RESET.

AD_0 – AD_7 (Input/Output, 3-state)
Multiplexed Address/Data Bus: Lower 8 bits of the memory address (or I/O address) appear on the bus during the first clock cycle (T state) of a machine cycle. It then becomes the data bus during the second and third clock cycles.

ALE (Output)
Address Latch Enable: It occurs during the first clock state of a machine cycle and enables the address to get latched into the on-chip latch of peripherals. The falling edge of ALE is set to guarantee setup and hold times for the address information. The falling edge of ALE can also be used to strobe the status information. ALE is never 3-stated.

S_0, S_1 and IO/$\overline{M}$
Machine cycle status:

IO/$\overline{M}$	S_1	S_0	States	IO/$\overline{M}$	S_1	S_0	States
0	0	1	Memory write	1	1	1	Interrupt Acknowledge
0	1	0	Memory read	.	0	0	Halt . =3-state
1	0	1	I/O write	.	x	x	Hold (high impedance)
1	1	0	I/O read	.	x	x	Reset x=unspecified
0	1	1	Opcode fetch				

S_1 can be used as an advanced R/W status. IO/$\overline{M}$, S_0 and S_1 become valid at the beginning of a machine cycle and remain stable throughout the cycle. The falling edge of ALE may be used to latch the state of these lines.

$\overline{\text{RD}}$ (Output, 3-state)
READ control: A low level on $\overline{\text{RD}}$ indicates the selected memory or I/O device is to be read and that the Data Bus is available for the data transfer, 3-stated during Hold and Halt modes and during RESET.

$\overline{\text{WR}}$ (Output, 3-state)
WRITE control: A low level on $\overline{\text{WR}}$ indicates the data on the Data Bus is to be written into the selected memory or I/O location. Data is set up at the trailing edge of WR, 3-stated during Hold and Halt modes and during RESET.

$\overline{\text{READY}}$ (Input)
If READY is high during a read or write cycle, it indicates that the memory or peripheral is ready to send or receive data. If READY is low, the CPU will wait an integral number of clock cycles for READY to go high before completing the read or write cycle. READY must conform to specified setup and hold times.

HOLD (Input)
HOLD indicates that another master is requesting the use of the address and data buses. The CPU, upon receiving the hold request, will relinquish the use of the bus as soon as the completion of the current bus transfer. Internal processing can continue. The processor can regain the bus only after the HOLD is removed. When the HOLD is acknowledged, the Address, Data, $\overline{\text{RD}}$, $\overline{\text{WR}}$, and IO/$\overline{\text{M}}$ lines are 3-stated.

HLDA (Output)
HOLD ACKNOWLEDGE: Indicates that the CPU has received the HOLD request and that it will relinquish the bus in the next clock cycle. HLDA goes low after the Hold request is removed. The CPU takes the bus one half clock cycle after HLDA goes low.

INTR (Input)
INTERRUPT REQUEST: Is used as a general purpose interrupt. It is sampled only during the next to the last clock cycle of an instruction and during Hold and Halt states. If it is active, the Program Counter (PC) will be inhibited from incrementing and an $\overline{\text{INTA}}$ will be issued. During this cycle a RESTART or CALL instruction can be inserted to jump to the interrupt service routine. The INTR is enabled and disabled by software. It is disabled by Reset and immediately after an interrupt is accepted.

$\overline{\text{INTA}}$ (Output)
INTERRUPT ACKNOWLEDGE: Is used instead of (and has the same timing as) $\overline{\text{RD}}$ during the instruction cycle after an INTR is accepted.

RST 5.5, RST 6.5, RST 7.5 (Input)
RESTART INTERRUPTS: These three inputs have the same timing as INTR except they cause an internal RESTART to be automatically inserted.

The priority of these interrupts is ordered as shown in Table C-1. These interrupts have a higher priority than INTR. In addition, they may be individually masked out using the SIM instruction.

TRAP (Input)
Trap interrupt is a nonmaskable RESTART interrupt. It is recognized at the same timing as INTR or RST 5.5 – 7.5. It is unaffected by any mask or Interrupt Disable. It has the highest priority of any interrupt. (See Table C-1.)

$\overline{\text{RESET IN}}$ (Input)
Sets the Program Counter to zero and resets the Interrupt Enable and HLDA flip-flops. The data and address buses and the control lines are 3-stated during RESET and because of the asynchronous nature of RESET, the processor's internal registers and flags may be altered by RESET with unpredictable results. RESET IN is a Schmitt-triggered input, allowing connection to an R-C network for power-on RESET delay. The CPU is held in the reset condition as long as $\overline{\text{RESET IN}}$ is applied.

RESET OUT (Output)
Indicates CPU is being reset. Can be used as a system reset. The signal is synchronized to the processor clock and lasts an integral number of clock periods.

X_1, X_2 (Input)
X_1 and X_2 are connected to a crystal to drive the internal clock generator. X_1 can also be an external clock input from a logic gate. The input frequency is divided by 2 to give the processor's internal operating frequency.

CLK (Output)
Clock Output for use as a system clock. The period of CLK is twice the X_1, X_2 input period.

SID (Input)
Serial input data line. The data on this line is loaded into accumulator bit 7 whenever a RIM instruction is executed.

SOD (Output)
Serial output data line. The output SOD is set or reset as specified by the SIM instruction.

Vcc
+5 volt supply.

GND
Ground Reference.

Name	Priority	Address Branched To (1) When Interrupt Occurs	Type Trigger
TRAP	1	24H	Rising edge and high level until sampled.
RST 7.5	2	3CH	Rising edge (latched).
RST 6.5	3	34H	High level until sampled.
RST 5.5	4	2CH	High level until sampled.
INTR	5	(2)	High level until sampled.

Notes: (1) The processor pushes the PC on the stack before branching to the indicated address.
(2) The address branched depends on the instruction provided to the CPU when the interrupt is acknowledged.

Table C-1. Interrupt Priority, Restart Address and Sensitivity

Function

The 80C85A has twelve addressable 8-bit registers. Four of them can function only as two 16-bit register pairs. Six others can be used interchangeably as 8-bit registers or a 16-bit register pairs. The 80C85A register set is as follows:

Mnemonic	Register	Contents
ACC or A	Accumulator	8-bits
PC	Program Counter	16-bit address
BC, DE, HL	General-Purpose Register; data pointer (HL)	8-bit $\times$ 6 or 16-bits $\times$ 3
SP	Stack Pointer	16-bit address
Flags or F	Flag Register	5 flag (8-bit space)

The 80C85A uses a multiplexed Data Bus. The address is split between the higher 8-bit Address Bus and the lower 8-bit Address/Data Bus. During the first T state (clock cycle) of a machine cycle the low order address is sent out on the Address/Data Bus. These lower 8-bits may be latched externally by the Address Latch Enable signal (ALE). During the rest of the machine cycle the data bus is used for memory or I/O data.

The 80C85A provides $\overline{RD}$, $\overline{WR}$, S_0, S_1 and IO/$\overline{M}$ signals for bus control. An Interrupt Acknowledge signal (INTA) is also provided. Hold and all Interrupts are synchronized with the processor's internal clock. The 80C85A also provides Serial Input Data (SID) and Serial Output Data (SOD) lines for a simple serial interface.

In addition to these features, 80C85A has three maskable, vector interrupt pins and one nonmaskable TRAP interrupt.

Interrupt and Serial I/O

The 80C85A has 5 interrupt inputs: INTR, RST 5.5, RST 6.5, RST 7.5, and TRAP. INTR is identical in function to the 8080A INT. Each of the three RESTART inputs, 5.5, 6.5, and 7.5, has a programmable mask. TRAP is also a RESTART interrupt but it is nonmaskable.

The three maskable interrupts cause the internal execution of RESTART (saving the program counter in the stack and branching to the RESTART address) if the interrupts are enabled and if the interrupt mask is not set. The nonmaskable TRAP causes the internal execution of a RESTART vector independent of the state of the interrupt enable or masks. (See Table C-1.)

There are two different types of inputs in the restart interrupts. RST 5.5 and RST 6.5 are high level-sensitive like INTR (and INT on the 8080A) and are recognized with the same timing as INTR. RST 7.5 is rising edge-sensitive.

For RST 7.5, only a pulse is required to set an internal flip-flop which generates the internal interrupt request. The RST 7.5 request flip-flop remains set until the request is serviced. Then it is reset automatically. This flip-flop may also be reset by using the SIM instruction or by issuing a $\overline{\text{RESET IN}}$ to the 80C85A. The RST 7.5 internal flip-flop will be set by a pulse on the RST 7.5 pin even when the RST 7.5 interrupt is masked out.

The interrupts are arranged in a fixed priority that determines which interrupt is to be recognized if more than one is pending as follows: TRAP-highest priority. RST 7.5, RST 6.5, RST 5.5, INTR-lowest priority. This priority scheme does not take into account the priority of a routine that was started by a higher priority interrupt. RST 5.5 can interrupt an RST 7.5 routine if the interrupts are re-enabled before the end of the RST 7.5 routine.

The TRAP interrupt is useful for catastrophic events such as power failure or bus error. The TRAP input is recognized just as any other interrupt but has the highest priority. It is not affected by any flag or mask. The TRAP input is both edge and level sensitive. The TRAP input must go high and remain high until it is acknowledged. It will not be recognized again until it goes low, then high again. This avoids any false triggering due to noise or logic glitches. Figure C-3 illustrates the TRAP interrupt request circuitry within the 80C85A. Note that the servicing of any interrupt (TRAP, RST 7.5, RST 6.5, RST 5.5, INTR) disables all future interrupts (except TRAPs) until an EI instruction is executed.

The TRAP interrupt is special in that it disables interrupts, but preserves the previous interrupt enable status. Performing the first RIM instruction following a TRAP interrupt allows you to determine whether interrupts were enabled or disabled prior to the TRAP. All subsequent RIM instructions provide current interrupt enable status. Performing a RIM instruction following INTR or RST 5.5 − 7.5 will provide current Interrupt Enable status, revealing that Interrupts are disabled.

The serial I/O system is also controlled by the RIM and SIM instructions. SID is read by RIM, and SIM sets the SOD data.

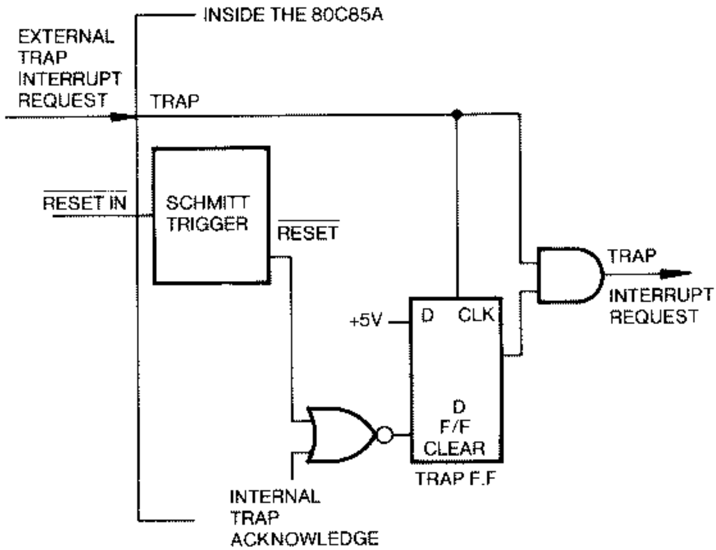


Figure C-3. Trap and $\overline{\text{RESET IN}}$

Basic System Timing

The 80C85A has a multiplexed Data Bus. ALE is used as a strobe to sample the lower 8-bits of address on the Data Bus. Figure C-4 shows an instruction fetch, memory read and I/O write cycle (as would occur during processing of the OUT instruction). Note that during the I/O write and read cycle that the I/O port address is copied on both the upper and lower half of the address.

There are seven possible types of machine cycles. Which of these seven takes place is defined by the status of the three status lines (IO/$\overline{M}$, S_1, S_0) and the three control signals ($\overline{RD}$, $\overline{WR}$, and $\overline{INTA}$). (See Table C-2.) The status line can be used as advanced controls (for device selection, for example), since they become active at the T_1 state, at the outset of each machine cycle. Control lines $\overline{RD}$ and $\overline{WR}$ become active later, at the time when the transfer of data is to take place, so are used as command lines.

A machine cycle normally consists of three T states, with the exception of OPCODE FETCH, which normally has either four or six T states (unless WAIT or HOLD states are forced by the receipt of $\overline{READY}$ or HOLD inputs). Any T state must be one of ten possible states, shown in Table C-3.

Machine Cycle	Status			Control		
	$IO/\overline{M}$	S_1	S_0	$\overline{RD}$	$\overline{WR}$	$\overline{INTA}$
Opcode Fetch (OF)	0	1	1	0	1	1
Memory Read (MR)	0	1	0	0	1	1
Memory Write (MW)	0	0	1	1	0	1
I/O Read (IOR)	1	1	0	0	1	1
I/O Write (IOW)	1	0	1 *	1	0	1
Acknowledge of INTR (INA)	1	1	1	1	1	0
Bus Idle (BI): DAD	0	1	0	1	1	1
ACK. OF RST, TRAP	1	1	1	1	1	1
HALT	TS	0	0	TS	TS	1

Table C-2. 80C85A Machine Cycle Chart

Machine State	Status & Buses				Control		
	S_1, S_0	$IO/\overline{M}$	$A_8 - A_{15}$	$AD_0 - AD_7$	$\overline{RD}, \overline{WR}$	$\overline{INTA}$	ALE
T_1	X	X	X	X	1	1	1 (1)
T_2	X	X	X	X	X	X	0
T_{WAIT}	X	X	X	X	X	X	0
T_3	X	X	X	X	X	X	0
T_4	1	0 (2)	X	TS	1	1	0
T_5	1	0 (2)	X	TS	1	1	0
T_6	1	0 (2)	X	TS	1	1	0
T_{RESET}	X	TS	TS	TS	TS	1	0
T_{HALT}	0	TS	TS	TS	TS	1	0
T_{HOLD}	X	TS	TS	TS	TS	1	0

0 = Logic "0"
1 = Logic "1"
TS = High Impedance
X = Unspecified

Notes : (1) ALE not generated during 2nd and 3rd machine cycles of DAD instruction.
(2) $IO/\overline{M}$ = 1 during $T_4 - T_6$ of INA machine cycle.

Table C-3. 80C85A Machine State Chart

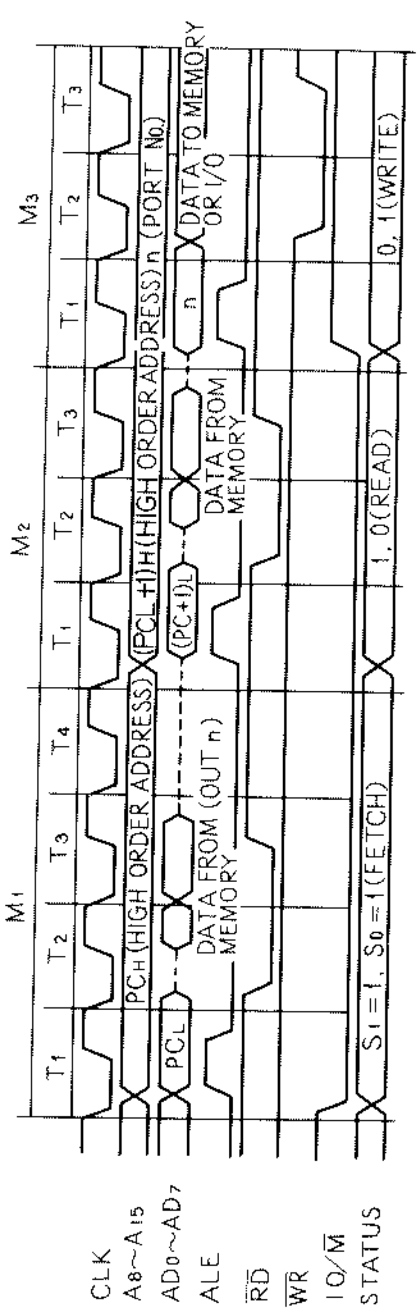


Figure C-4. 80C85A Basic System Timing

81C55

General Description

The MSM81C55RS/GS is a 2K bit static RAM (256 byte) with parallel I/O ports. It uses silicon gate CMOS technology and consumes a standby current of 100 micro ampere maximum while the chip is not selected. Featuring a maximum access time of 400 ns, the MSM81C55RS/GS can be used in an 80C85A system without using wait states. The parallel I/O consists of two 8-bit ports and one 6-bit port (both general purpose). The MSM81C55RS/GS also contains a 14-bit programmable counter/timer which may be used for sequence-wave generation or terminal countpulsing.

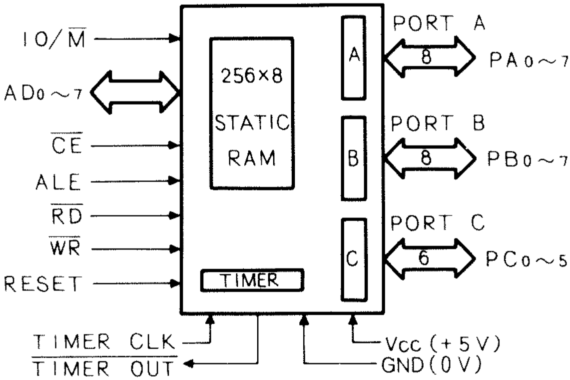


Figure C-5. Functional Block Diagram

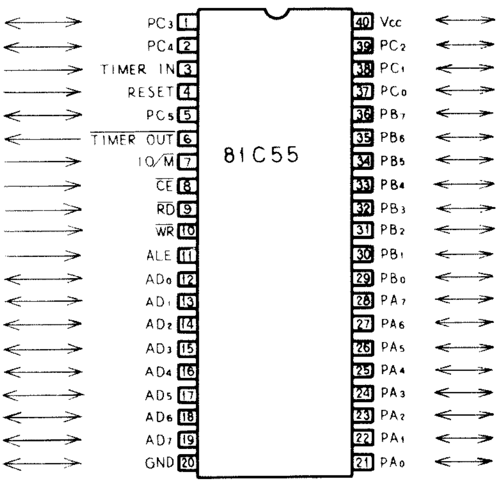


Figure C-6. Pin Configuration of 81C55

Functional Pin Description

RESET (Input)
A high level input to this pin resets the chip, placing all three I/O ports in the input mode, and stops timer.

ALE (Input)
Negative going edge of the ALE (Address Latch Enable) input latches AD_{0-7}, IO/M, and CE signals into the respective latches.

AD_{0-7} (Input/Output)
Three-state, bi-directional address/data bus. Eight-bit address information on this bus is read into the internal address latch at the negative going edge of the ALE. Eight bits of data can be read from or written to the chip using this bus depending on the state of the WRITE or READ input.

$\overline{CE}$ (Input)
When the CE input is high, both read and write operations to the chip are disabled.

IO/$\overline{M}$ (Input)
A high level input to this pin selects the internal I/O functions, and a low level selects the memory.

$\overline{RD}$ (Input)
If this pin in low, data from either the memory or ports is read onto the AD_{0-7} lines depending on the state of the IO/$\overline{M}$ line.

$\overline{WR}$ (Input)
If this pin is low, data on lines AD_{0-7} is written into either the memory or into the selected port depending on the state of the IO/$\overline{M}$ line.

PA_{0-7}, PB_{0-7} (Input/Output)
General-purpose I/O pins. Input/output directions can be determined by programming the command/status (C/S) register.

PC_{0-5} (Input/Output)
Three pins are usable either as general-purpose I/O pins or control pins for the PA and PB ports. When used as control pins, they are assigned to the following functions:
PC0: A INTR (port A interrupt)
PC1: A BF (port A full)
PC2: A $\overline{STB}$ (port A strobe)
PC3: B INTR (port B interrupt)
PC4: B BF (port B buffer full)
PC5: B $\overline{STB}$ (port B strobe)

TIMER IN (Input)
Input to the counter/timer

$\overline{\text{TIMER OUT}}$ (Output)
Timer output. When the present count is reached during timer operation, this pin provides a square-wave or pulse output depending on the programmed control status.

Function

81C55 has 3 functions as described below.

- 2K bit static RAM (256 words × 8 bits)
- Two 8-bit I/O ports (PA and PB) and a 6-bit I/O port (PC)
- 14-bit timer counter

The internal register is shown in the figure below, and the I/O addresses are described in the table below.

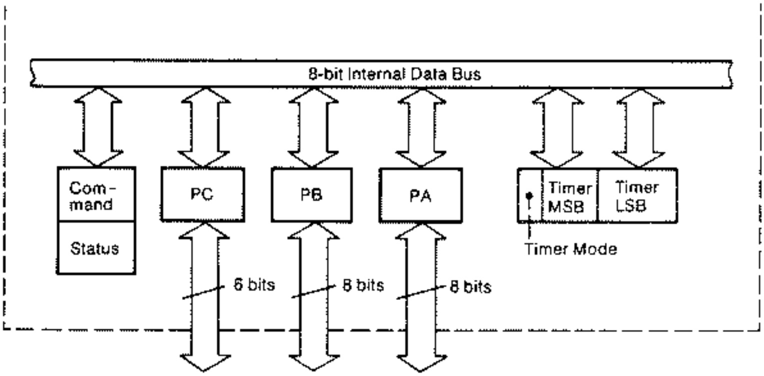


Figure C-7. Internal Register of 81C55

I/O Address								Selecting Register
A7	A6	A5	A4	A3	A2	A1	A0	
X	X	X	X	X	0	0	0	Internal command/status register
X	X	X	X	X	0	0	1	Universal I/O port A (PA)
X	X	X	X	X	0	1	0	Universal I/O port B (PB)
X	X	X	X	X	0	1	1	I/O port C (PC)
X	X	X	X	X	1	0	0	Timer count lower position 8 bits (LSB)
X	X	X	X	X	1	0	1	Timer count upper position 6 bits and timer mode 2 bits (MSB)

X : Don't care.

Table C-4. I/O Address of 81C55

(1) Programming the Command/Status (C/S) Register

The contents of the command register can be written during an I/O cycle by addressing it with an I/O address of xxxxx000. Bit assignments for the register are shown below:

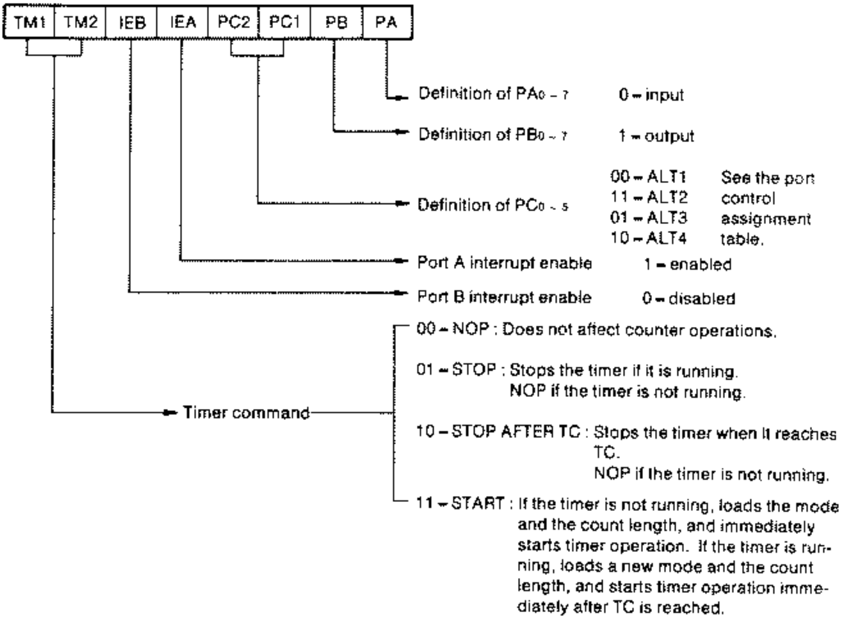


Figure C-8. Programming the Command/Status Register

Pin	ALT1	ALT2	ALT3	ALT4
PC_0	Input port	Output port	A INTR	A INTR
PC_1	Input port	Output port	A BF	A BF
PC_2	Input port	Output port	A STB	A STB
PC_3	Input port	Output port	Output port	B INTR
PC_4	Input port	Output port	Output port	B BF
PC_5	Input port	Output port	Output port	B STB

Table C-5. Port Control Assignment

(2) Reading the C/S Register

The I/O and timer status can be accessed by reading the contents of the Status register located at I/O address xxxxx000. The status word format is shown below:

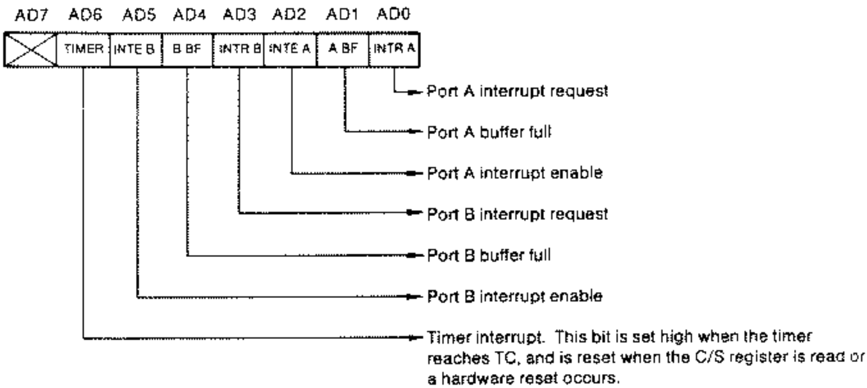


Figure C-9. Reading the C/S Register

(3) PA and PB Registers

These registers may be used as either input or output ports depending on the programmed contents of the C/S register. They may also be used either in the basic mode or in the strobe mode.

I/O address of the PA register: xxxxx001
I/O address of the PB register: xxxxx010

(4) PC Register

The PC register may be used as an input port, output port or control register depending on the programmed contents of the C/S register. The I/O address of the PC register is xxxxx011.

(5) Timer

The timer is a 14-bit counter which counts TIMER IN pulses.

The low order byte of the timer register has an I/O address of xxxxx100, and the high order byte of the register has an I/O address of xxxxx101.

The count length register (CLR) may be preset with two bytes of data. Bits 0 through 13 are assigned to the count length: bits 14 and 15 specify the timer output mode. A read operation of the CLR reads the contents of the counter and the pertinent output mode. The initial value range which can initially be loaded into the counter is 2 through 3FFF hex. Bit assignments to the timer counter and possible output modes are shown in the following.

M2	M1	T13	T12	T11	T10	T9	T8

Output mode High order 6 bits of count length

T7	T6	T5	T4	T3	T2	T1	T0

Low order byte of count length

Figure C-10. Bit Assignments to the Timer Counter

M_2	M_1	
0	0	Outputs a low-level signal in the latter half (Note 1) of a count period.
0	1	Outputs a low-level signal in the latter half of a count period, automatically loads the programmed count length, and restarts counting when the TC value is reached.
1	0	Outputs a pulse when the TC value is reached.
1	1	Outputs a pulse each time the preset TC value is reached, automatically loads the programmed count length, and restarts from the beginning.

Note 1: When counting an asymmetrical value such as (9), a high level is output during the first period of five, and a low level is output during the second period of four.

Note 2: If an internal counter of the 81C55 receives a reset signal, count operation stops but the counter is not set to a specific initial value or output mode. When restarting count operation after reset, the START command must be executed again through the C/S register.

(6) Standby Mode

The 81C55 is placed in standby mode when the high level at $\overline{CE}$ input is latched during the negative going edge of ALE. All input ports and the timer input should be pulled up or down to either Vcc or GND potential.

When using battery back-up, all ports should be set low or in input port mode. The timer output should be set low. Otherwise, a buffer should be added to the timer output and the battery should be connected to the power supply pins of the buffer.

By setting the reset input to a high level, the standby mode can be selected. In this case, the command register is reset, so the ports automatically set to the input mode and the timer stops.

82C51A

General Description

82C51A is USART (Universal Synchronous Asynchronous Receiver Transmitter) for serial data communication developed for the microcomputer system.

As a peripheral device of the microcomputer system, 82C51A receives parallel data from CPU and transmits serial data after conversion. This device also receives serial data from outside and transmits parallel data to CPU after conversion. Thus the device is used for serial data communication.

82C51A configures a fully static circuit using silicon gate CMOS technology. Therefore, it operates on an extremely low power supply at 100 μA (max.) of standby current by suspending all the operations. 82C51A is functionally compatible with 8251A.

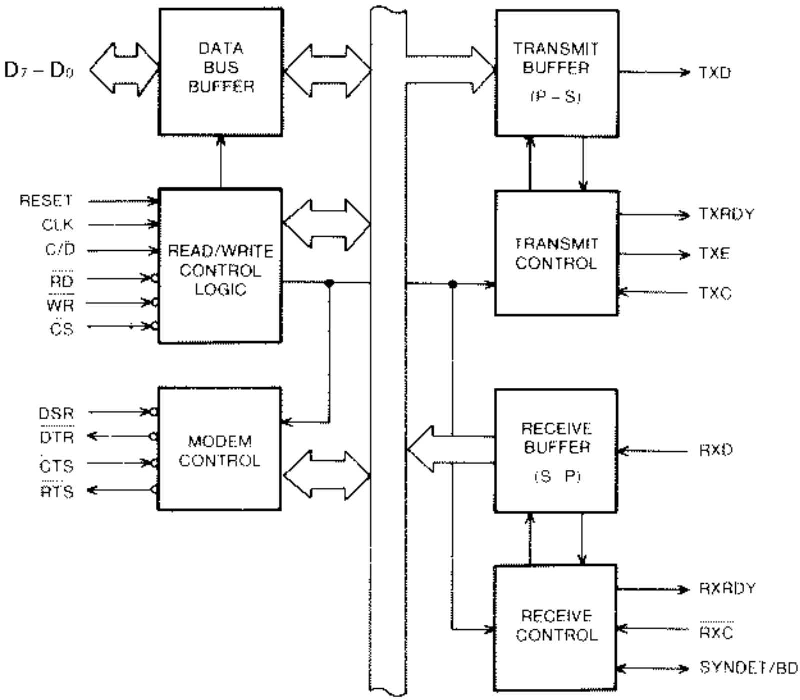


Figure C-11. Functional Block Diagram

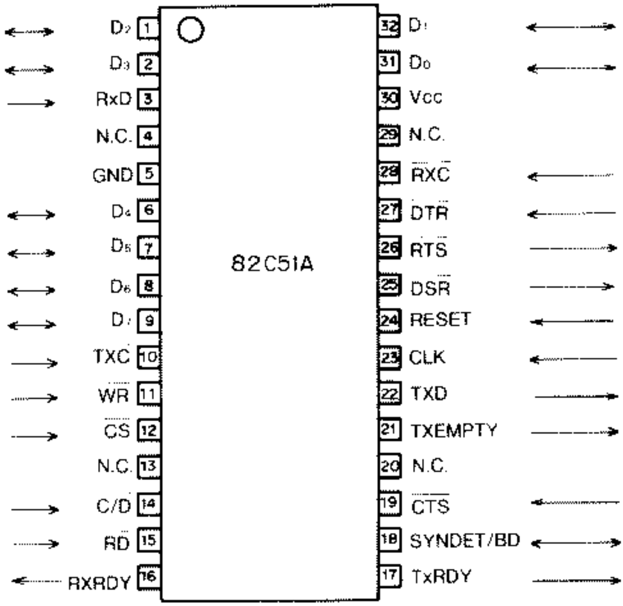


Figure C-12. Pin Configuration of 82C51A

Functional Pin Description

D_0 – D_7 (Input/Output)
This is a bidirectional data bus which receives control word and transmit data from CPU and sends status word and received data to CPU.

RESET (Input)
A "High" on this input forces the 82C51A into "reset status".

The device waits for the writing of "mode instruction".

The min. reset width is six clock inputs during the operating status of CLK.

CLK (Input)
CLK signal is used to generate an internal device timing.

CLK signal is independent of $\overline{\text{RXC}}$ or $\overline{\text{TXC}}$.

However, the frequency of CLK must be greater than 30 times the $\overline{\text{RXC}}$ and $\overline{\text{TXC}}$ at Synchronous mode and Asynchronous "x1" mode, and must be greater than 5 times at Asynchronous "x16" and "x64" mode.

$\overline{\text{WR}}$ (Input)
This is "active low" input terminal which receives a signal for waiting transmit data and control words from CPU into 82C51A.

$\overline{\text{RD}}$ (Input)
This is "active low" input terminal which receives a signal for reading receive data and status words from 82C51A.

C/$\overline{D}$ (Input)
This is an input terminal which receives a signal for selecting data or command word and status word when 82C51A is accessed by CPU.

If C/$\overline{D}$ = low, data will be accessed.
If C/$\overline{D}$ = high, command word or status word will be accessed.

$\overline{CS}$ (Input)
This is "active low" input terminal which selects the 82C51A at low level when CPU accesses.

> **Note:** The device won't be in "standby status" only setting $\overline{CS}$ = High. Refer to "Standby Status".

TXD (Output)
This is an output terminal for transmit data from which serial-converted data is sent out.

The device is in "mark status" (high level) after resetting or during a status when transmit is disabled.

It is also possible to set the device in "break status" (low level) by a command.

TXRDY (Output)
This is an output terminal which indicates that 82C51A is ready to accept a transmit data character.

But the terminal is always at low level if $\overline{CTS}$ = high or the device was set in "TX disable status" by a command.

> **Note:** TXRDY of status word indicates that transmit data character is receivable, regardless of $\overline{CTS}$ or command.

If CPU write a data character, TXRDY will be reset by the leading edge or $\overline{WR}$ signal.

TXEMPTY (Output)
This is an output terminal which indicates that 82C51A transmitted all the characters and had no data character.

In "synchronous mode", the terminal is at high level, if transmit data characters are no longer left and sync characters are automatically transmitted.

If CPU write a data character, TXEMPTY will be reset by the leading edge of $\overline{WR}$ signal.

> **Note:** As a transmitter is disabled by setting $\overline{CTS}$ "High" or command, a data written before disabled will be sent out, then TXD and TXEMPTY will be "High". Even if a data is written after disable, that data is not sent out and TXE will be "High".
> After enabled transmitter, it is sent out.

$\overline{TXC}$ (Input)
This is a clock input signal which determines the transfer speed of transmit data.

In "synchronous mode", the baud rate will be the same as the frequency of $\overline{TXC}$.

In "asynchronous mode", it is possible to select baud rate factor by mode instruction. It can be 1, 1/16 or 1/64 the TXC.

The falling edge of $\overline{\text{TXC}}$ shifts the serial data out of the 82C51A.

RXD (Input)
This is a terminal which receives serial data.

RXRDY (Output)
This is a terminal which indicates that 82C51A contains a character that is ready to READ.

If CPU reads a data character, RXRDY will be reset by the leading edge of $\overline{\text{RD}}$ signal.

Unless CPU reads a data character before next one character is received completely, the preceding data will be lost. In such a case, an overrun error flag of status word will be set.

$\overline{\text{RXC}}$ (Input)
This is a clock input signal which determines the transfer speed of receive data.

In "synchronous mode", the baud rate will be the same as the frequency of $\overline{\text{RXC}}$.

In "asynchronous mode", it is possible to select baud rate factor by mode instruction. It can be 1, 1/16, 1/64 the $\overline{\text{RXC}}$.

SYNDET/BD (Input/Output)
This is a terminal which function changes according to mode.

In "internal synchronous mode", this terminal is at high level, if sync characters are received and synchronized. If status word is read, the terminal will be reset.

In "external synchronous mode", this is an input terminal.

If "High" on this input forces, 82C51A starts receiving data character.

In "asynchronous mode", this is an output terminal which generates "high level" output upon the detection of "break" character, if receiver data contained "low level" space between stop bits of two continuous characters. The terminal will be reset, if RXD is at high level.

$\overline{\text{DSR}}$ (Input)
This is an input port for MODEM interface. The input status of the terminal can be recognized by CPU reading status words.

$\overline{\text{DTR}}$ (Output)
This is an output port for MODEM interface. It is possible to set the status of $\overline{\text{DTR}}$ by a command.

$\overline{\text{CTS}}$ (Input)
This is an input terminal for MODEM interface which is used for controlling a transmit circuit. The terminal controls data transmit if the device is set in "TX Enable" status by a command.

Data is transmittable if the terminal is at low level.

$\overline{\text{RTS}}$ (Output)
This is an output port for MODEM interface. It is possible to set the status of $\overline{\text{RTS}}$ by a command.

Function

Outline

82C51A's functional configuration is programmed by the software.

Operation between 82C51A and CPU is executed by program control. Table C-6 shows the operation between CPU and the device.

$\overline{CS}$	$C/\overline{D}$	$\overline{RD}$	$\overline{WR}$	
1	X	X	X	Data bus 3-state
0	X	1	1	Data bus 3-state
0	1	0	1	Status → CPU
0	1	1	0	Control word ← CPU
0	0	0	1	Data → CPU
0	0	1	0	Data ← CPU

Table C-6. Operation between 82C51A and CPU

It is necessary to execute a function-setting sequence after resetting on 82C51A. Figure C-13 shows the function-setting sequence.

If the function was set, the device is ready to receive a command, thus enabling the transfer of data by setting a necessary command, reading a status and reading/writing data.

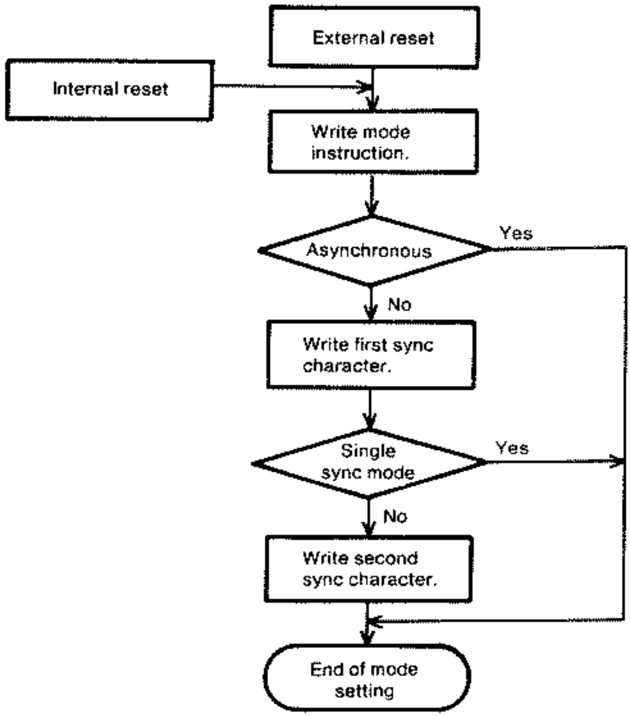


Figure C-13. Function-Setting Sequence (Mode Instruction Sequence)

There are two types of control words.
1. Mode instruction (setting of function)
2. Command (setting of operation)

1. Mode Instruction
Mode instruction is used for setting the function of 82C51A. Mode instruction will be in "wait for write" at either internal reset or external reset. That is, the writing of control word after resetting will be recognized as "mode instruction".

Items to be set by mode instruction are as follows:
- Synchronous/Asynchronous mode
- Character hronous mode
- Character length
- Parity bit
- Baud rate factor (asynchronous mode)
- Internal/external synchronization (synchronous mode)
- No. of synchronous characters (synchronous mode)

The bit configuration of mode instruction is shown in Figures C-14 and C-15. In the case of synchronous mode, it is necessary to write one- or two-type sync characters.

If sync characters were written, a function will be set because the writing of sync characters constitutes part of mode instruction.

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
S_2	S_1	EP	PEN	L_2	L_1	B_2	B_1

Baud rate factor

0	1	0	1
0	0	1	1
Refer to Fig. C-15	1x	16x	64x

Character length

0	1	0	1
0	0	1	1
5 bits	6 bits	7 bits	8 bits

Parity check

0	1	0	1
0	0	1	1
Disable	Odd parity	Disable	Even parity

Stop bit length

0	1	0	1
0	0	1	1
Inhibit	1 bit	1.5 bits	2 bits

Figure C-14. Bit Configuration of Mode Instruction (Asynchronous)

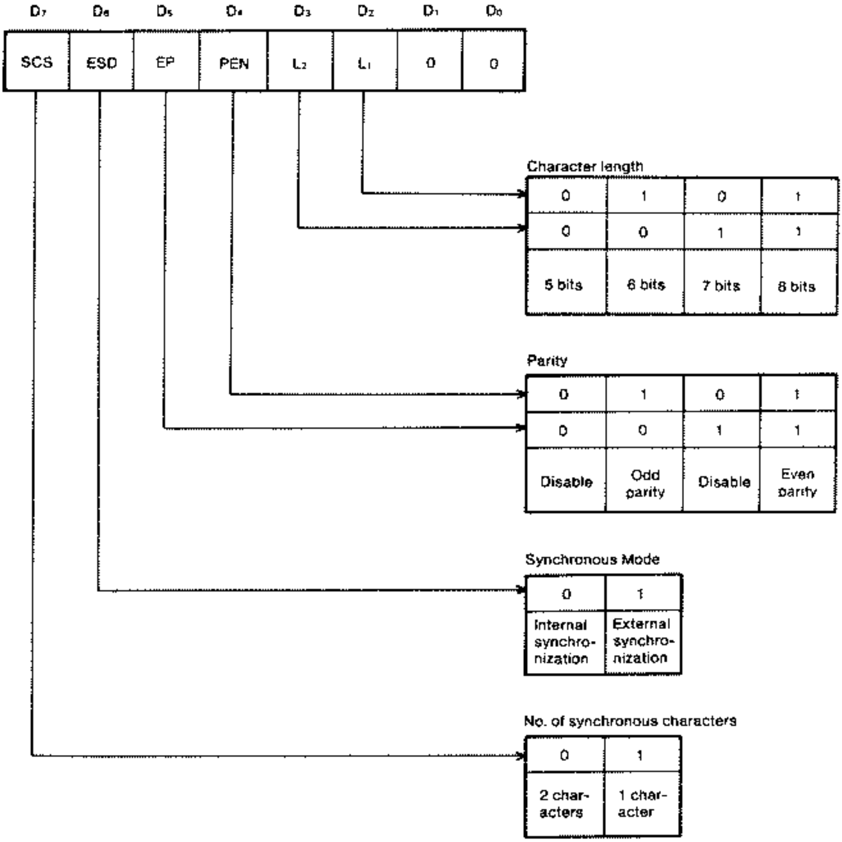


Figure C-15. Bit Configuration of Mode Instruction (Synchronous)

2. Command

Command is used for setting the operation of 82C51A.

It is possible to write a command whenever necessary after writing mode instruction and sync characters.

Items to be set by command are as follows:

- Transmit   Enable/Disable
- Receive   Enable/Disable
- $\overline{DTR}$, $\overline{RTS}$ Output of data
- Resetting of error flag
- Sending of break characters
- Internal resetting
- Hunt mode (synchronous mode)

The bit configuration of a command is shown in Figure C-16.

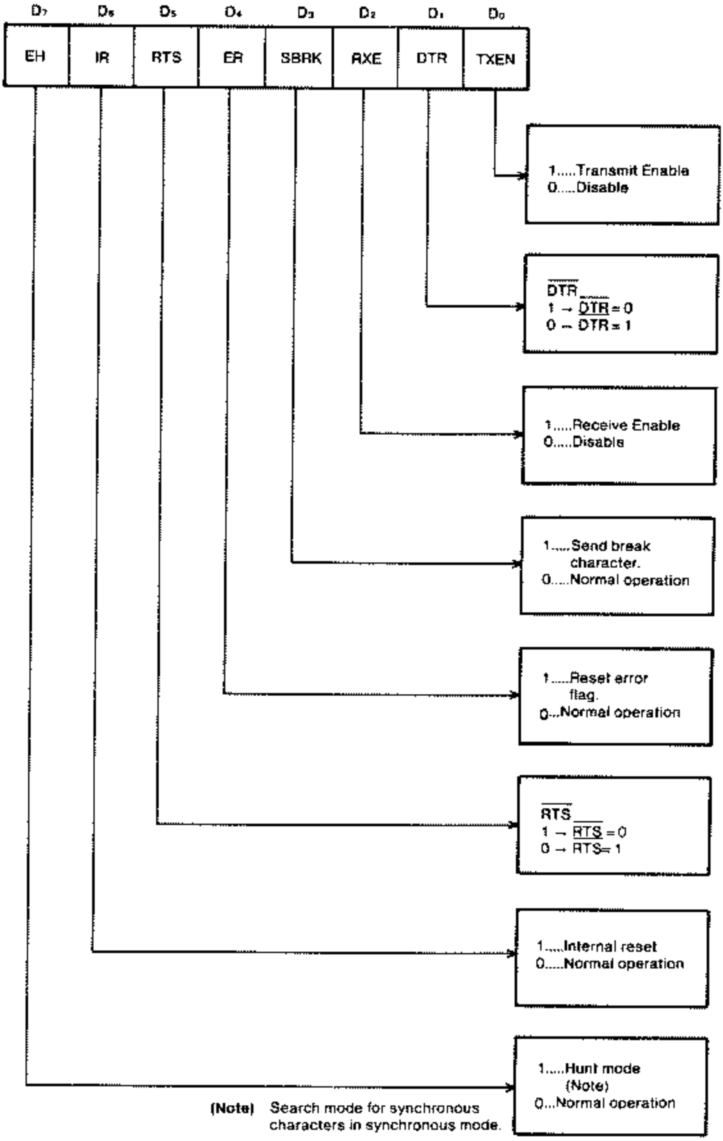


Figure C-16. Bit Configuration of Command

Status Word

It is possible to see the internal status of 82C51A by reading a status word. The bit configuration of status word is shown in Figure C-17.

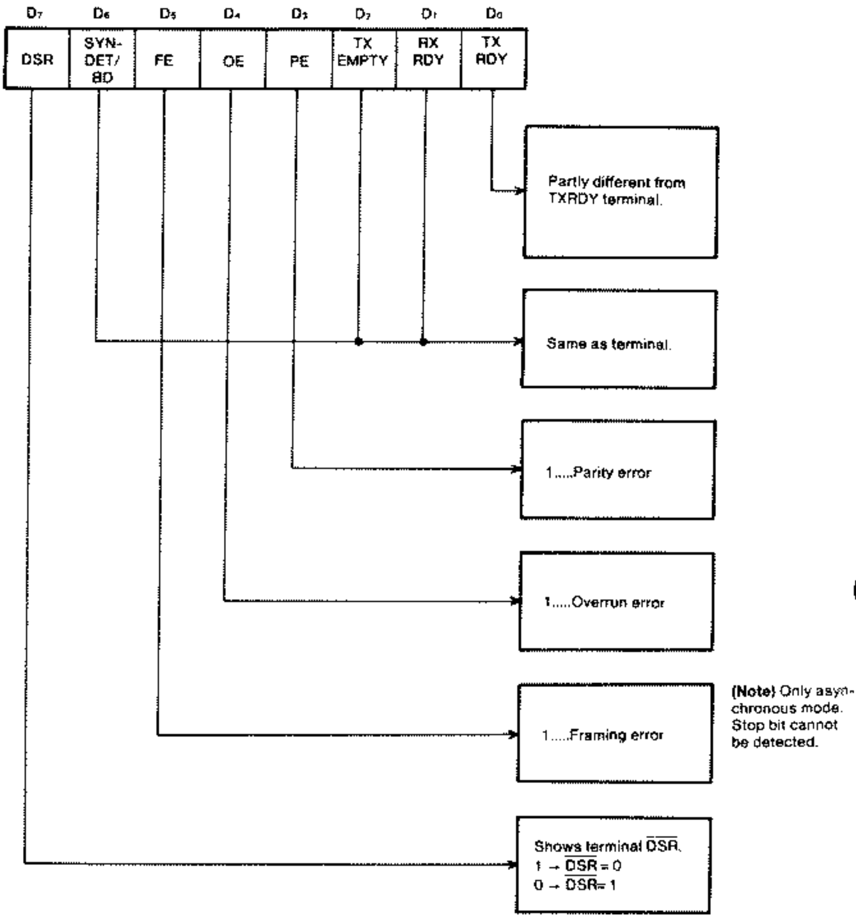


Figure C-17. Bit Configuration of Status Word

Standby Status

It is possible to put 82C51A in "standby status" for the complete static configuration of CMOS.

When the following conditions have been satisfied that 82C51A is in "standby status".

- $\overline{CS}$ terminal shall be fixed at VCC level.
- Input pins other than $\overline{CS}$, D0 to D7, $\overline{RD}$, $\overline{WR}$ and C/$\overline{D}$ shall be fixed at VCC or GND level (including SYNDET in external synchronous mode).

Note: When all outputs current are 0, ICCS specification is applied.

Basic Construction of LCD

Liquid crystal is a substance midway between a liquid and a solid, although its appearance is much like a liquid. From an electrical and optical standpoint, it possesses the properties of a crystal. Items which use this substance are called liquid crystal display elements. The LCD used in the Tandy 200 is a TN (Twisted Nematic) type of liquid crystal. Its basic construction is shown in Figure C-18.

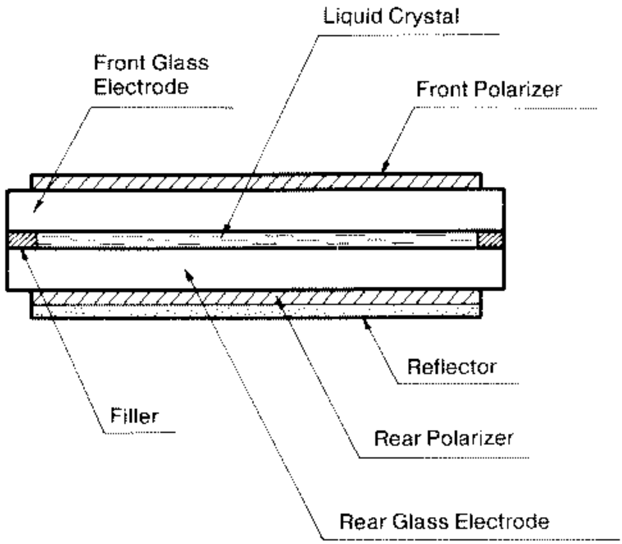


Figure C-18. Construction of LCD Panel

The LCD operates as an "electric shutter" that controls the passage of light.

If voltage is applied, the transmission of light is blocked, otherwise, light is allowed to pass so that letters and numbers can be displayed.

Figure C-19 demonstrates how the LCD operates:

- The liquid-crystal display element is sandwiched between the two polarization plates. The polarized axes of the upper and lower plates are placed at right angles to each other to use the optical "twisting" of light.
- As shown in Figure C-19 (a), if voltage is not applied, the liquid-crystal molecules between the upper and lower plates twist 90° to distribute light. This results in a 90° optical movement and the transmission of light.
- In Figure C-19 (b), however, voltage is applied and the liquid appears frosted in current-carrying areas, thus blocking light transmission.

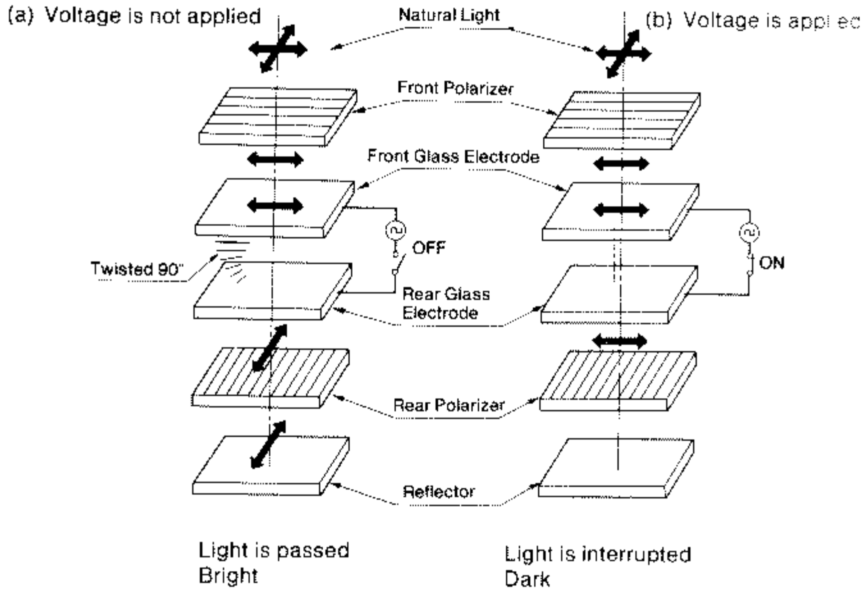


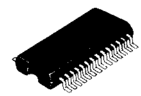
Figure C-19. Operation Theory of LCD Panel

HM6264LFP-12,HM6264LFP-15

8192-word x 8-bit High Speed Static CMOS RAM

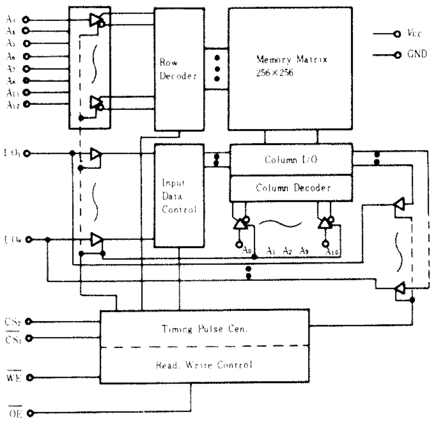
■ FEATURES

- High Density Small-sized Packaged
- Projection Area Reduced to One-Thirds of Conventional DIP
- Thickness Reduced to a Half of Conventional DIP
- High Speed: Fast Access Time 120/150ns (max)
- Single 5V Supply
- Low Power Standby and Low Power Operation
  Standby: 10μW (typ.), Operation: 200mW (typ.)
- Capability of Battery Back-up Operation
- Completely Static RAM: No clock nor Timing Strobe Required
- Directly TTL Compatible: All Input and Output
- Equal Access and Cycle Time

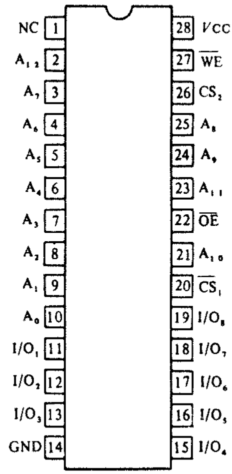


(FP-28)

■ BLOCK DIAGRAM



■ PIN ARRANGEMENT



(Top View)

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Terminal Voltage *	V_T	−0.5 ** to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C
Storage Temperature (Under Bias)	T_{bias}	−10 to +85	°C

* With respect to GND. ** Pulse width 50ns: −3.0V

■ TRUTH TABLE

$\overline{WE}$	$\overline{CS_1}$	CS_2	$\overline{OE}$	Mode	I/O Pin	V_{CC} Current	Note
X	H	X	X	Not Selected (Power Down)	High Z	I_{SB}, I_{SB1}	
X	X	L	X		High Z	I_{SB}, I_{SB2}	
H	L	H	H	Output Disabled	High Z	I_{CC}, I_{CC1}	
H	L	H	L	Read	Dout	I_{CC}, I_{CC1}	
L	L	H	H	Write	Din	I_{CC}, I_{CC1}	Write Cycle (1)
L	L	H	L		Din	I_{CC}, I_{CC1}	Write Cycle (2)

X: H or L

■ RECOMMENDED DC OPERATING CONDITIONS (T_a = 0 to +70°C)

Item	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	GND	0	0	0	V
Input Voltage	V_{IH}	2.2	–	6.0	V
	V_{IL}	-0.3*	–	0.8	V

* Pulse Width 50ns: -3.0V

■ DC AND OPERATING CHARACTERISTICS (V_{CC} = 5V±10%, GND = 0V, T_a = 0 to +70°C)

Item	Symbol	Test Condition	min	typ*	max	Unit
Input Leakage Current	$\|I_{LI}\|$	V_{in}=GND to V_{CC}	–	–	2	μA
Output Leakage Current	$\|I_{LO}\|$	$\overline{CS1}=V_{IH}$ or $CS2=V_{IL}$ or $\overline{OE}=V_{IH}$ or $\overline{WE}=V_{IL}$, $V_{I/O}$=GND or V_{CC}	–	–	2	μA
Operating Power Supply Current	I_{CC}	$\overline{CS1}=V_{IL}$, $CS2=V_{IH}$, $I_{I/O}$=0mA	–	40	80	mA
Average Operating Current	I_{CC1}	Min. cycle, duty=100%, $I_{I/O}$=0mA	–	60	110	mA
Standby Power Supply Current	I_{SB}	$\overline{CS1}=V_{IH}$ or $CS2=V_{IL}$	–	1	3	mA
	I_{SB1}**	$\overline{CS1} \geq V_{CC}-0.2V$, $CS2 \geq V_{CC}-0.2V$ or $CS2 \leq 0.2V$	–	2	100	μA
	I_{SB2}**	$CS2 \leq 0.2V$	–	2	100	μA
Output Voltage	V_{OL}	I_{OL}=2.1mA	–	–	0.4	V
	V_{OH}	I_{OH}=-1.0mA	2.4	–	–	V

* Typical limits are at V_{CC}=5.0V, T_a=25°C and specified loading.
** V_{IL} min=-0.3V

■ CAPACITANCE (f = 1MHz, T_a = 25°C)

Item	Symbol	Test Condition	typ	max	Unit
Input Capacitance	C_{in}	V_{in} = 0V	–	6	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$ = 0V	–	8	pF

Note) This parameter is sampled and not 100% tested.

■ AC CHARACTERISTICS (V_{CC} = 5V±10%, Ta = 0 to +70°C)

• AC TEST CONDITIONS

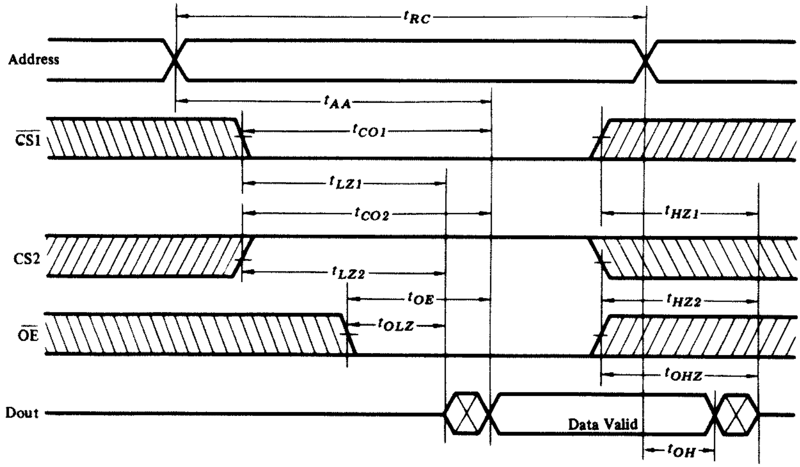
Input Pulse Levels: 0.8 to 2.4V
Input Rise and Fall Times: 10ns
Input and Output Timing Reference Level: 1.5V
Output Load: 1TTL Gate and C_L = 100pF (including scope and jig)

• READ CYCLE

Item		Symbol	HM6264LFP-12		HM6264LFP-15		Unit
			min	max	min	max	
Read Cycle Time		t_{RC}	120	–	150	–	ns
Address Access Time		t_{AA}	–	120	–	150	ns
Chip Selection to Output	$\overline{CS1}$	t_{CO1}	–	120	–	150	ns
	CS2	t_{CO2}	–	120	–	150	ns
Output Enable to Output Valid		t_{OE}	–	60	–	70	ns
Chip Selection to Output in Low Z	$\overline{CS1}$	t_{LZ1}	10	–	15	–	ns
	CS2	t_{LZ2}	10	–	15	–	ns
Output Enable to Output in Low Z		t_{OLZ}	5	–	5	–	ns
Chip Deselection to Output in High Z	$\overline{CS1}$	t_{HZ1}	0	40	0	50	ns
	CS2	t_{HZ2}	0	40	0	50	ns
Output Disable to Output in High Z		t_{OHZ}	0	40	0	50	ns
Output Hold from Address Change		t_{OH}	10	–	15	–	ns

NOTES: 1 t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit condition and are not referred to output voltage levels.
2 At any given temperature and voltage condition, t_{HZ} max is less than t_{LZ} min both for a given device and from device to device.

• **READ CYCLE**

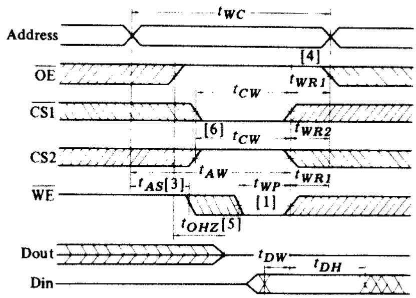


NOTE : 1) $\overline{WE}$ is high for Read Cycle

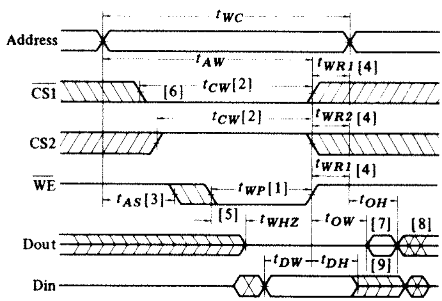
• **WRITE CYCLE**

Item		Symbol	HM6264LFP-12		HM6264LFP-15		Unit
			min	max	min	max	
Write Cycle Time		t_{WC}	120	–	150	–	ns
Chip Selection to End of Write		t_{CW}	85	–	100	–	ns
Address Setup Time		t_{AS}	0	–	0	–	ns
Address Valid to End of Write		t_{AW}	85	–	100	–	ns
Write Pulse Width		t_{WP}	70	–	90	–	ns
Write Recovery Time	$\overline{CS1}$, $\overline{WE}$	t_{WR1}	5	–	10	–	ns
	CS2	t_{WR2}	15	–	15	–	ns
Write to Output in High Z		t_{WHZ}	0	40	0	50	ns
Data to Write Time Overlap		t_{DW}	50	–	60	–	ns
Data Hold from Write Time		t_{DH}	0	–	0	–	ns
OE to Output in High Z		t_{OHZ}	0	40	0	50	ns
Output Active from End of Write		t_{OW}	5	–	10	–	ns

• WRITE CYCLE (1) ($\overline{OE}$ clock)



• WRITE CYCLE (2) ($\overline{OE}$ Low Fix)



NOTES:

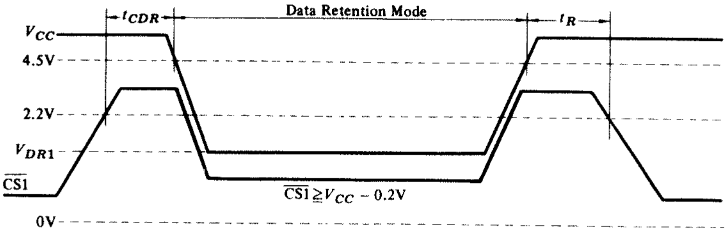
1) A write occurs during the overlap of a low $\overline{CS1}$, a high CS2 and a low $\overline{WE}$. A write begins at the latest transition among $\overline{CS1}$ going low, CS2 going high and $\overline{WE}$ going low. A write ends at the earliest transtion among $\overline{CS1}$ going high, CS2 going low and $\overline{WE}$ going high. t_{WP} is measured from the beginninng of write to the end of write.
2) t_{CW} is measured from the later of $\overline{CS1}$ going low or CS2 going high to the end of write.
3) t_{AS} is measured from the address valid to the beginning of write.
4) t_{WR} is measured from the end of write to the address change. t_{WR1} applies in case a write ends at $\overline{CS1}$ or $\overline{WE}$ going high. t_{WR2} applies in case a write ends at CS2 going low.
5) During this period, I/O pins are in the output state, therefore the input signals of opposite phase to the outputs must not be applied.
6) If $\overline{CS1}$ goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low, the outputs remain in high impedance state.
7) Dout is the same phase of the latest written data in this write cycle.
8) Dout is the read data of next address.
9) If $\overline{CS1}$ is low and CS2 is high during this period, I/O pins are in the output state. Therefore, the input signals of opposite phase to the outputs must not be applied to them.

■ LOW V_{CC} DATA RETENTION CHARACTERISTICS (T_a = 0 to +70 °C)

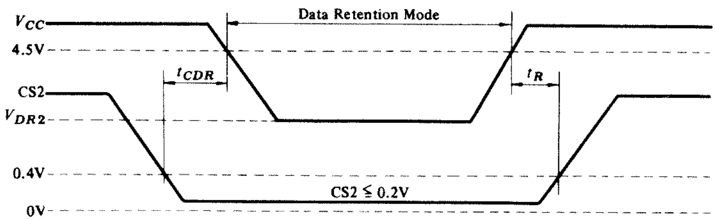
Item	Symbol	Test Condition	min	typ	max	Unit
V_{CC} for Data Retention	V_{DR1}	$\overline{CS1} \geq V_{CC} - 0.2V$, $CS2 \geq V_{CC} - 0.2V$ or $CS2 \leq 0.2V$	2.0	–	–	V
	V_{DR2}	$CS2 \leq 0.2V$	2.0	–	–	V
Data Retention Current	I_{CCDR1}	$V_{CC} = 3.0V$, $\overline{CS1} \geq V_{CC} - 0.2V$, $CS2 \geq V_{CC} - 0.2V$ or $CS2 \leq 0.2V$	–	1	50*	μA
	I_{CCDR2}	$V_{CC} = 3.0V$, $CS2 \leq 0.2V$	–	1	50*	μA
Chip Deselect to Data Retention Time	t_{CDR}	See Retention Waveform	0	–	–	ns
Operation Recovery Time	t_R		t_{RC}**	–	–	ns

* V_{IL} min = −0.3V, 20μA max at T_a=0 ~ 40°C.
** t_{RC} = Read Cycle Time

• LOW Vcc DATA RETENTION WAVEFORM (1) ($\overline{CS1}$ Controlled)



• LOW Vcc DATA RETENTION WAVEFORM (2) (CS2 Controlled)



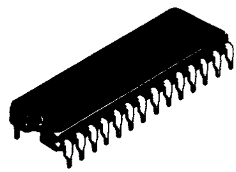
NOTE: In Data Retention Mode, CS2 controls the Address, $\overline{WE}$, $\overline{CS1}$, $\overline{OE}$ and Din buffer. If CS2 controls data retention mode, Vin for these inputs can be in the high impedance state. If $\overline{CS1}$ controls the data retention mode, CS2 must satisfy either CS2 ≥ Vcc−0.2V or CS2 ≤ 0.2V. The other input levels (address, $\overline{WE}$, $\overline{OE}$, I/O)can be in the high impedance state.

HM6264LP-10, HM6264LP-12
HM6264LP-15

8192-word x 8-bit High Speed Static CMOS RAM

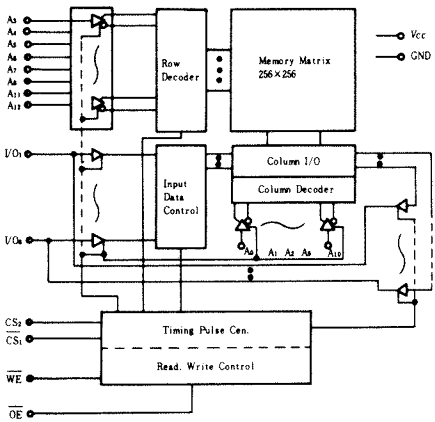
■ FEATURES

- Fast access Time 100ns/120ns/150ns (max.)
- Low Power Standby Standby: 0.01mW (typ.)
  Low Power Operation Operating: 200mW (typ.)
- Capability of Battery Back-up Operation
- Single +5V Supply
- Completely Static Memory. . . . . No clock or Timing Strobe Required
- Equal Access and Cycle Time
- Common Data Input and Output, Three State Output
- Directly TTL Compatible: All Input and Output
- Standard 28pin Package Configuration
- Pin Out Compatible with 64K EPROM HN482764

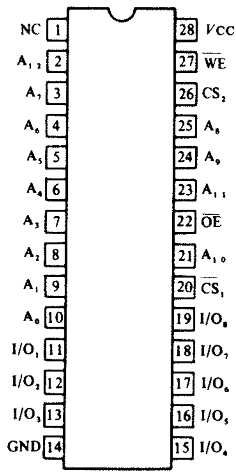


(DP-28)

■ BLOCK DIAGRAM



■ PIN ARRANGEMENT



(Top View)

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Terminal Voltage *	V_T	−0.5 ** to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C
Storage Temperature (Under Bias)	T_{bias}	−10 to +85	°C

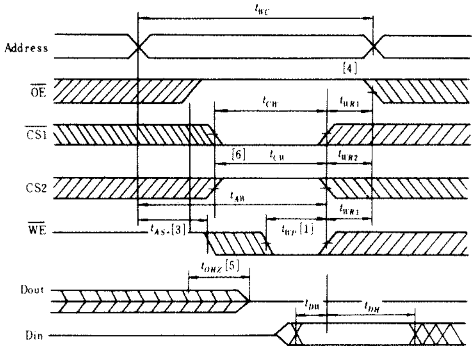
* With respect to GND. ** Pulse width 50ns: −3.0V

■ TRUTH TABLE

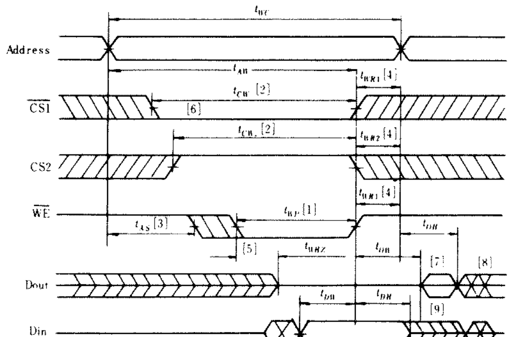
$\overline{WE}$	$\overline{CS_1}$	CS_2	$\overline{OE}$	Mode	I/O Pin	V_{CC} Current	Note
X	H	X	X	Not Selected (Power Down)	High Z	I_{SB}, I_{SB1}	
X	X	L	X		High Z	I_{SB}, I_{SB2}	
H	L	H	H	Output Disabled	High Z	I_{CC}, I_{CC1}	
H	L	H	L	Read	Dout	I_{CC}, I_{CC1}	
L	L	H	H	Write	Din	I_{CC}, I_{CC1}	Write Cycle (1)
L	L	H	L		Din	I_{CC}, I_{CC1}	Write Cycle (2)

X: H or L

• **WRITE CYCLE (1) ($\overline{OE}$ clock)**



• **WRITE CYCLE (2) ($\overline{OE}$ Low Fix)**



NOTES:
1) A write occurs during the overlap of a low $\overline{CS1}$, a high CS2 and a low $\overline{WE}$. A write begins at the latest transition among $\overline{CS1}$ going low, CS2 going high and $\overline{WE}$ going low. A write ends at the earliest transition among $\overline{CS1}$ going high, CS2 going low and $\overline{WE}$ going high. t_{WP} is measured from the beginninng of write to the end of write.
2) t_{CW} is measured from the later of $\overline{CS1}$ going low or CS2 going high to the end of write.
3) t_{AS} is measured from the address valid to the beginning of write.
4) t_{WR} is measured from the end of write to the address change. t_{WR1} applies in case a write ends at $\overline{CS1}$ or $\overline{WE}$ going high. t_{WR2} applies in case a write ends at CS2 going low.
5) During this period, I/O pins are in the output state, therefore the input signals of opposite phase to the outputs must not be applied.
6) If $\overline{CS1}$ goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low, the outputs remain in high impedance state.
7) Dout is the same phase of the latest written data in this write cycle.
8) Dout is the read data of next address.
9) If $\overline{CS1}$ is low and CS2 is high during this period, I/O pins are in the output state. Therefore, the input signals of opposite phase to the outputs must not be applied to them.

■ RECOMMENDED DC OPERATING CONDITIONS (T_a = 0 to +70°C)

Item	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	GND	0	0	0	V
Input Voltage	V_{IH}	2.2	–	6.0	V
	V_{IL}	–0.3*	–	0.8	V

* Pulse Width 50ns: –3.0V

■ DC AND OPERATING CHARACTERISTICS (V_{CC} = 5V±10%, GND = 0V, T_a = 0 to +70°C)

Item	Symbol	Test Condition	min	typ*	max	Unit
Input Leakage Current	$\|I_{LI}\|$	V_{in}=GND to V_{CC}	–	–	2	μA
Output Leakage Current	$\|I_{LO}\|$	$\overline{CS1}=V_{IH}$ or $CS2=V_{IL}$ or $\overline{OE}=V_{IH}$ or $\overline{WE}=V_{IL}$, $V_{I/O}$=GND to V_{CC}	–	–	2	μA
Operating Power Supply Current	I_{CC}	$\overline{CS1}=V_{IL}$, $CS2=V_{IH}$, $I_{I/O}$=0mA	–	40	80	mA
Average Operating Current	I_{CC1}	Min. cycle, duty=100%, $I_{I/O}$=0mA	–	60	110	mA
Standby Power Supply Current	I_{SB}	$\overline{CS1}=V_{IH}$ or $CS2=V_{IL}$	–	1	3	mA
	I_{SB1}**	$\overline{CS1} \geqq V_{CC}-0.2V$, $CS2 \geqq V_{CC}-0.2V$ or $CS2 \leqq 0.2V$	–	2	100	μA
	I_{SB2}**	$CS2 \leqq 0.2V$	–	2	100	μA
Output Voltage	V_{OL}	I_{OL}=2.1mA	–	–	0.4	V
	V_{OH}	I_{OH}=–1.0mA	2.4	–	–	V

* Typical limits are at V_{CC}=5.0V, T_a=25°C and specified loading.
** V_{IL} min=–0.3V

■ CAPACITANCE (f= 1MHz, T_a = 25°C)

Item	Symbol	Test Condition	typ	max	Unit
Input Capacitance	C_{in}	V_{in} = 0V	–	6	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$ = 0V	–	8	pF

Note) This parameter is sampled and not 100% tested.

■ AC CHARACTERISTICS (V_{CC} = 5V±10%, Ta = 0 to +70°C)

• AC TEST CONDITIONS

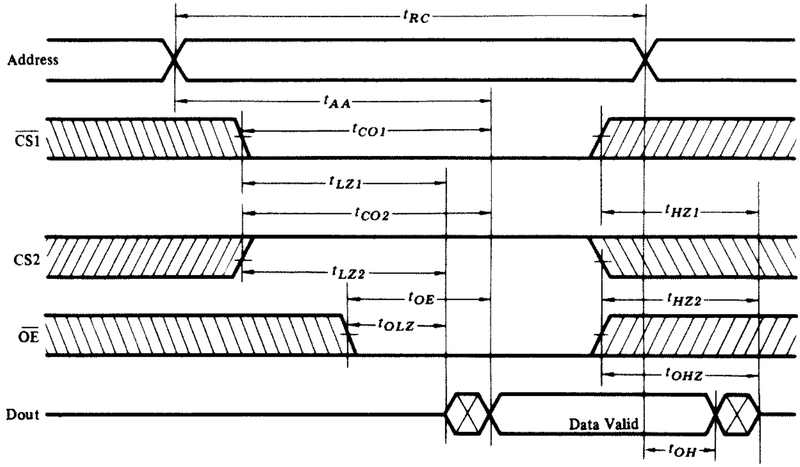
Input Pulse Levels: 0.8 to 2.4V
Input Rise and Fall Times: 10ns
Input and Output Timing Reference Level: 1.5V
Output Load: 1TTL Gate and C_L = 100pF (including scope and jig)

• READ CYCLE

Item		Symbol	HM6264LP-10		HM6264LP-12		HM6264LP-15		Unit
			min	max	min	max	min	max	
Read Cycle Time		t_{RC}	100	–	120	–	150	–	ns
Address Access Time		t_{AA}	–	100	–	120	–	150	ns
Chip Selection to Output	$\overline{CS1}$	t_{CO1}	–	100	–	120	–	150	ns
	CS2	t_{CO2}	–	100	–	120	–	150	ns
Output Enable to Output Valid		t_{OE}	–	50	–	60	–	70	ns
Chip Selection to Output in Low Z	$\overline{CS1}$	t_{LZ1}	10	–	10	–	15	–	ns
	CS2	t_{LZ2}	10	–	10	–	15	–	ns
Output Enable to Output in Low Z		t_{OLZ}	5	–	5	–	5	–	ns
Chip Deselection to Output in High Z	$\overline{CS1}$	t_{HZ1}	0	35	0	40	0	50	ns
	CS2	t_{HZ2}	0	35	0	40	0	50	ns
Output Disable to Output in High Z		t_{OHZ}	0	35	0	40	0	50	ns
Output Hold from Address Change		t_{OH}	10	–	10	–	15	–	ns

NOTES: 1 t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit condition and are not referred to output voltage levels.
2 At any given temperature and voltage condition, t_{HZ} max is less than t_{LZ} min both for a given device and from device to device.

• **READ CYCLE**

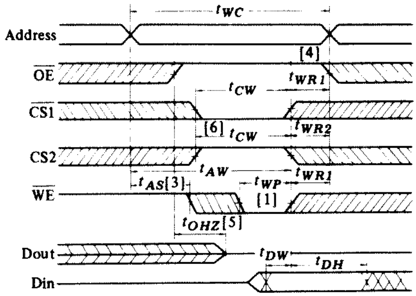


NOTE : 1) $\overline{WE}$ is high for Read Cycle

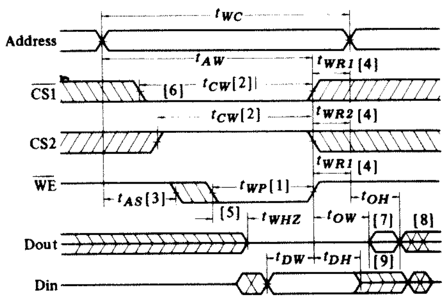
• **WRITE CYCLE**

Item		Symbol	HM6264LP-10		HM6264LP-12		HM6264LP-15		Unit
			min	max	min	max	min	max	
Write Cycle Time		t_{WC}	100	–	120	–	150	–	ns
Chip Selection to End of Write		t_{CW}	80	–	85	–	100	–	ns
Address Setup Time		t_{AS}	0	–	0	–	0	–	ns
Address Valid to End of Write		t_{AW}	80	–	85	–	100	–	ns
Write Pulse Width		t_{WP}	60	–	70	–	90	–	ns
Write Recovery Time	$\overline{CS1}$, $\overline{WE}$	t_{WR1}	5	–	5	–	10	–	ns
	CS2	t_{WR2}	15	–	15	–	15	–	ns
Write to Output in High Z		t_{WHZ}	0	35	0	40	0	50	ns
Data to Write Time Overlap		t_{DW}	40	–	50	–	60	–	ns
Data Hold from Write Time		t_{DH}	0	–	0	–	0	–	ns
$\overline{OE}$ to Output in High Z		t_{OHZ}	0	35	0	40	0	50	ns
Output Active from End of Write		t_{OW}	5	–	5	–	10	–	ns

• **WRITE CYCLE (1) ($\overline{OE}$ clock)**



• **WRITE CYCLE (2) ($\overline{OE}$ Low Fix)**



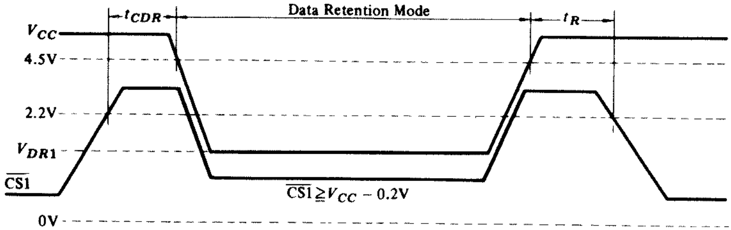
NOTES:
1) A write occurs during the overlap of a low $\overline{CS1}$, a high CS2 and a low $\overline{WE}$. A write begins at the latest transition among $\overline{CS1}$ going low, CS2 going high and $\overline{WE}$ going low. A write ends at the earliest transtion among $\overline{CS1}$ going high, CS2 going low and $\overline{WE}$ going high. t_{WP} is measured from the beginninng of write to the end of write.
2) t_{CW} is measured from the later of $\overline{CS1}$ going low or CS2 going high to the end of write.
3) t_{AS} is measured from the address valid to the beginning of write.
4) t_{WR} is measured from the end of write to the address change. t_{WR1} applies in case a write ends at $\overline{CS1}$ or $\overline{WE}$ going high. t_{WR2} applies in case a write ends at CS2 going low.
5) During this period, I/O pins are in the output state, therefore the input signals of opposite phase to the outputs must not be applied.
6) If $\overline{CS1}$ goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low, the outputs remain in high impedance state.
7) Dout is the same phase of the latest written data in this write cycle.
8) Dout is the read data of next address.
9) If $\overline{CS1}$ is low and CS2 is high during this period, I/O pins are in the output state. Therefore, the input signals of opposite phase to the outputs must not be applied to them.

■ LOW V_{CC} DATA RETENTION CHARACTERISTICS (T_a = 0 to +70 °C)

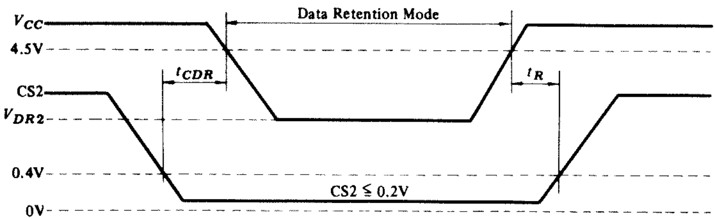
Item	Symbol	Test Condition	min	typ	max	Unit
V_{CC} for Data Retention	V_{DR1}	$\overline{CS1} \geq V_{CC} - 0.2V, CS2 \geq V_{CC} - 0.2V$ or $CS2 \leq 0.2V$	2.0	–	–	V
	V_{DR2}	$CS2 \leq 0.2V$	2.0	–	–	V
Data Retention Current	I_{CCDR1}	$V_{CC} = 3.0V, \overline{CS1} \geq V_{CC} - 0.2V$, $CS2 \geq V_{CC} - 0.2V$ or $CS2 \leq 0.2V$	–	1	50*	μA
	I_{CCDR2}	$V_{CC} = 3.0V, CS2 \leq 0.2V$	–	1	50*	μA
Chip Deselect to Data Retention Time	t_{CDR}	See Retention Waveform	0	–	–	ns
Operation Recovery Time	t_R		t_{RC}**	–	–	ns

* V_{IL} min = −0.3V, 20μA max at T_a=0~40°C
** t_{RC} = Read Cycle Time

• LOW Vcc DATA RETENTION WAVEFORM (1) ($\overline{CS1}$ Controlled)

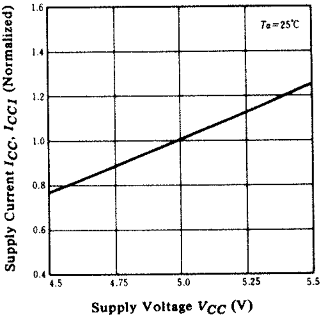


• LOW Vcc DATA RETENTION WAVEFORM (2) (CS2 Controlled)

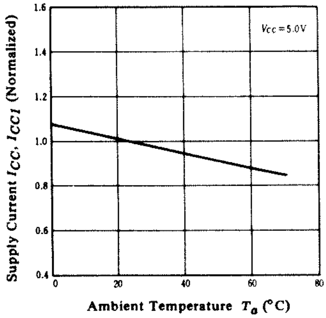


NOTE: In Data Retention Mode, CS2 controls the Address, $\overline{WE}$, $\overline{CS1}$, $\overline{OE}$ and Din buffer. If CS2 controls data retention mode, Vin for these inputs can be in the high impedance state. If $\overline{CS1}$ controls the data retention mode, CS2 must satisfy either CS2 $\geq$ Vcc−0.2V or CS2 $\leq$ 0.2V. The other input levels (address, $\overline{WE}$, $\overline{OE}$, I/O) can be in the high impedance state.

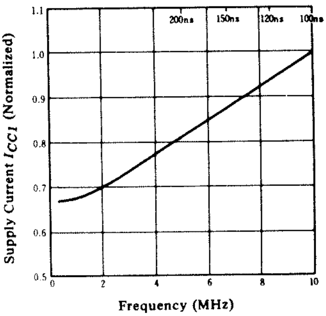
SUPPLY CURRENT vs. SUPPLY VOLTAGE



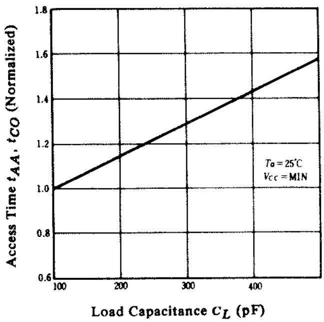
SUPPLY CURRENT vs. AMBIENT TEMPERATURE



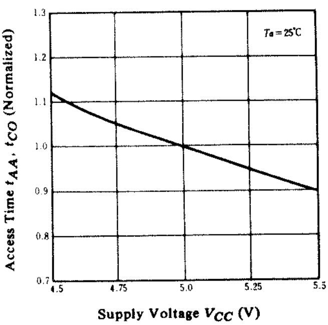
SUPPLY CURRENT vs. FREQUENCY



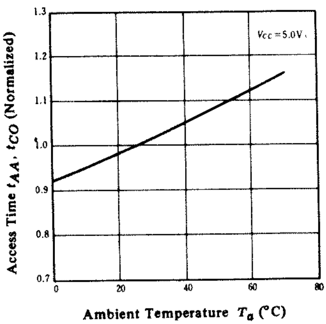
ACCESS TIME vs. LOAD CAPACITANCE



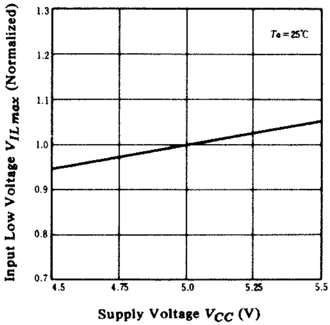
ACCESS TIME vs. SUPPLY VOLTAGE



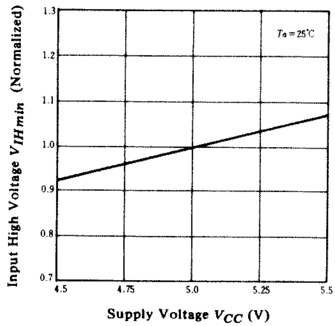
ACCESS TIME vs. AMBIENT TEMPERATURE



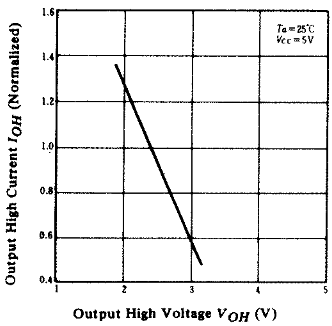
INPUT LOW VOLTAGE vs. SUPPLY VOLTAGE



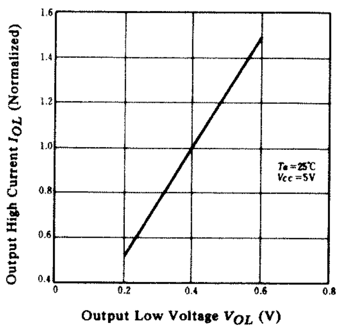
INPUT HIGH VOLTAGE vs. SUPPLY VOLTAGE



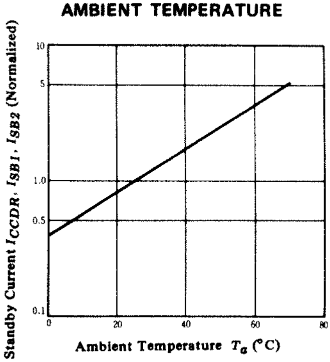
OUTPUT CURRENT vs. OUTPUT VOLTAGE



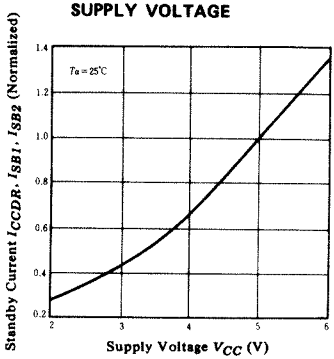
OUTPUT CURRENT vs. OUTPUT VOLTAGE



STANDBY CURRENT vs. AMBIENT TEMPERATURE



STANDBY CURRENT vs. SUPPLY VOLTAGE



HN613256P, HN613256FP

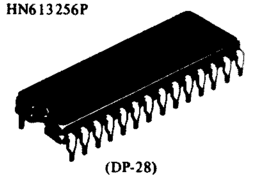
32768-word x 8-bit Mask Programmable Read Only Memory

The HN613256P/FP is a mask-programmable, byte-organized memory designed for use in bus-organized system.

To facilitate use, the device operates from a single power supply, has compatibility with TTL, and requires no clocks nor refreshing because of static operation.

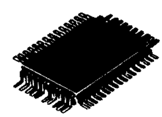
The active level of the CS and OE input, and the memory content are defined by the user. The Chip Select input deselects the output and puts the chip in a power-down mode.

HN613256P



(DP-28)

HN613256FP

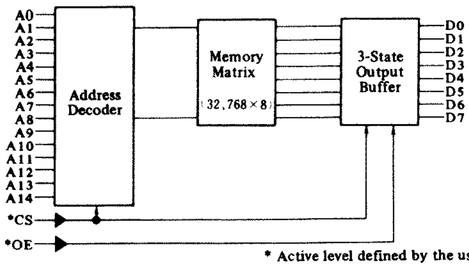


(FP-54)

■ FEATURES

- Fully Static Operation
- Automatic Power Down
- Single +5V Power Supply
- Three-state Data Output for OR-ties
- Mask Programmable Chip Select and Output Enable
- TTL Compatible
- Maximum Access Time: 250ns
- Low Power Standby and Low Power Operation; Standby 5μW (typ.), Operation 50mW (typ.)
- Pin Compatible with EPROM

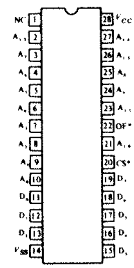
■ BLOCK DIAGRAM



* Active level defined by the user.

■ PIN ARRANGEMENT

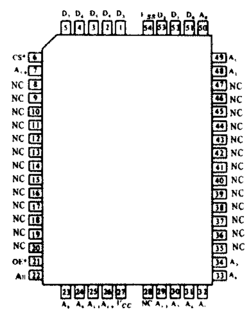
● HN613256P



(Top View)

* Active level can be defined by the customer.

● HN613256FP



(Top View)

* Active level can be defined by the customer.

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Supply Voltage*	V_{CC}	−0.3 to +7.0	V
Input Voltage*	V_{in}	−0.3 to +7.0	V
Operating Temperature Range	T_{opr}	−20 to +75	°C
Storage Temperature Range	T_{stg}	−55 to +125	°C
Storage Temperature Range (Under Bias)	T_{bias}	−20 to +85	°C

*With respect to V_{SS}

■ RECOMMENDED DC OPERATING CONDITIONS

Item	Symbol	min.	typ.	max.	Unit
Supply Voltage*	V_{CC}	4.5	5.0	5.5	V
Input Voltage*	V_{IL}	−0.3	−	0.8	V
	V_{IH}	2.2	−	V_{CC}	V
Operating Temperature	T_{opr}	−20	−	75	°C

* With respect to V_{SS}.

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Supply Voltage*	V_{CC}	$-0.3\sim+7.0$	V
Input Voltage*	V_{in}	$-0.3\sim+7.0$	V
Operating Temperature Range	T_{opr}	$0\sim+75$	℃
Storage Temperature Range	T_{stg}	$-55\sim+125$	℃
Bias Storage Temperature Range	T_{bias}	$-20\sim+85$	℃

Note : * Referenced to V_{SS}.

■ ELECTRICAL CHARACTERISTICS

($V_{CC}=5V\pm10\%$, $V_{SS}=0V$, $Ta=0\sim+75$℃)

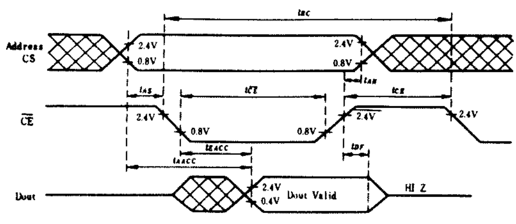
Item		Symbol	Test Condition		min	typ**	max	Unit
Input "High" Level Voltage		V_{IH}			2.4	—	V_{CC}	V
Input "Low" Level Voltage		V_{IL}			0	—	0.8	V
Output "High" Level Voltage		V_{OH}	$I_{OH}=-100\mu A$		2.4	—	—	V
Output "Low" Level Voltage		V_{OL}	$I_{OL}=1.6mA$		—	—	0.4	V
Input Leakage Current		I_{in}	$V_{in}=0\sim5.5V$		—	—	2.5	μA
Output "High" Level Leakage Current		I_{LOH}	$CE=0.8V$	$V_{out}=2.4V$	—	—	5	μA
Output "Low" Level Leakage Current		I_{LOL}	$\overline{CE}=2.4V$	$V_{out}=0.4V$	—	—	5	μA
Supply Current	In stand-by	I_{SB}	$\overline{CS}\geqq V_{CC}-0.2V$, $CS\geqq V_{SS}+0.2V$	$V_{CC}=5.5V$	—	1	30	μA
	In operation	I_{CC}*	$t_{RC}=4.0\mu s$, $I_{out}=0mA$, $t_{\overline{CE}}=3.0\mu s$		—	1.5	3.0	mA
Input Capacitance		C_{in}	$V_{in}=0V$, $f=1MHz$, $Ta=25$℃		—	—	10	pF
Output Capacitance		C_{out}			—	—	12.5	pF

* Steady state current ** $V_{CC}=5V$, $T_a=25$℃

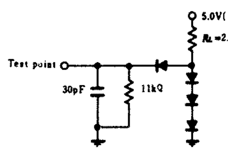
■ AC OPERATING CONDITION AND CHARACTERISTICS

● READ SEQUENCE ($V_{CC}=5V\pm10\%$, $V_{SS}=0V$, $Ta=0\sim+75$℃, $t_r=t_f=20ns$)

Item	Symbol	min	max	Unit
Read Cycle Time	t_{RC}	4.0	—	μs
Address Access Time	t_{AACC}	—	3.5	μs
Chip Enable Access Time	t_{EACC}	—	3.0	μs
Data Hold Time from Address	t_{DF}	0.05	0.5	μs
Address Set-up Time	t_{AS}	0.5	—	μs
Address Hold Time	t_{AH}	0	—	μs
Chip Enable ON Time	$t_{\overline{CE}}$	3.0	—	μs
Chip Enable OFF Time	t_{CE}	0.5	—	μs



● AC TEST LOAD



Notes : 1. $t_r=t_f=20ns$.
2. C_L includes jig capacitance.
3. All diodes are 1S2074Ⓗ.

■ ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0V±10%, V_{SS} = 0V, T_a = –20 ~ +75 °C)

Item		Symbol	Test Condition	min	typ**	max	Unit
Input Voltage		V_{IH}		2.2	–	V_{CC}	V
		V_{IL}		–0.3	–	0.8	V
Output Voltage		V_{OH}	I_{OH} = –205 μA	2.4	–	–	V
		V_{OL}	I_{OL} = 3.2 mA	–	–	0.4	V
Input Leakage Current		I_{in}	V_{in} = 0 ~ 5.5V	–	–	2.5	μA
Output Leakage Current		I_{LOH}	CS = 0.8V, $\overline{CS}$ = 2.2V, V_{out} = 2.4V	–	–	10	μA
		I_{LOL}	CS = 0.8V, $\overline{CS}$ = 2.2V, V_{out} = 0.4V	–	–	10	μA
Supply Current	Active	I_{CC}*	V_{CC} = 5.5V, I_{out} = 0mA, t_{RC} = min, duty = 100%.	–	10	30	mA
	Standby	I_{SB}	V_{CC} = 5.5V, $\overline{CS}$ ≥ V_{CC} – 0.2V, CS ≤ 0.2V	–	1	30	μA
Input Capacitance		C_{in}	V_{in} = 0V, f = 1 MHz, T_a = 25 °C	–	–	10	pF
Output Capacitance		C_{out}	V_{in} = 0V, f = 1 MHz, T_a = 25 °C	–	–	15	pF

* Steady state current
** V_{CC}=5V, T_a=25°C

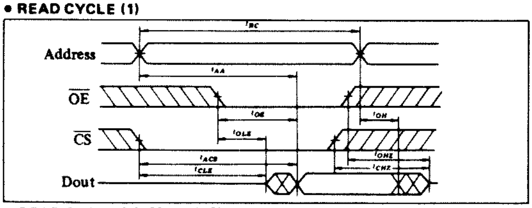
■ RECOMMENDED AC OPERATING CONDITIONS (READ SEQUENCE)

(V_{CC}=5V±10%, V_{SS}=0V, Ta= –20~+75°C, t_r=t_f=20ns)

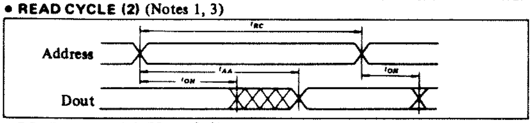
Item	Symbol	min	max	Unit
Read Cycle Time	t_{RC}	200	–	ns
Address Access Time	t_{AA}	–	200	ns
Chip Select Access Time	t_{ACS}	–	200	ns
Chip Selection to Output in Low Z	t_{CLZ}	10	–	ns
Output Enable to Output Valid	t_{OE}	–	100	ns
Output Enable to Output in Low Z	t_{OLZ}	10	–	ns
Chip Deselection to Output in High Z	t_{CHZ}	0	100	ns
Chip Disable to Output in High Z	t_{OHZ}	0	100	ns
Output Hold from Address Change	t_{OH}	10	–	ns

■ TIMING WAVEFORM

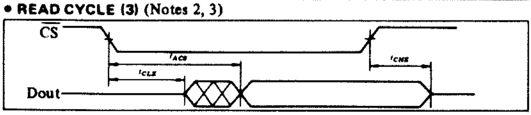
• READ CYCLE (1)



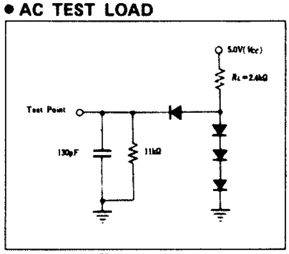
• READ CYCLE (2) (Notes 1, 3)



• READ CYCLE (3) (Notes 2, 3)



• AC TEST LOAD



Notes : 1. t_r=t_f=20ns
2. C_L includes jig capacitance
3. All diodes are 1S2074Ⓗ

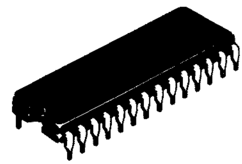
NOTES:
1. Device is continuously selected.
2. Address Valid prior to or coincident with $\overline{CS}$ transition low.
3. $\overline{OE}$ = V_{IL}.
4. Input pulse level: 0.8 to 2.4V
5. Input and output reference level: 1.5V

HN61364P, HN61364FP

8192-word x 8-bit Mask Programmable Read Only Memory

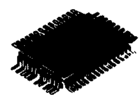
The HN61364P/FP is a mask-programmable, byte-organized memory designed for use in bus-organized systems.
To facilitate use, the device operates from a single power supply, has compatibility with TTL, and requires no clocks or refreshing because of static operation.
The active level of the CS, $OE_0 \sim OE_2$ inputs and the memory content are defined by the user. The Chip Select input deselects the output and puts the chip in a powerdown mode.

HN61364P



(DP-28)

HN61364FP

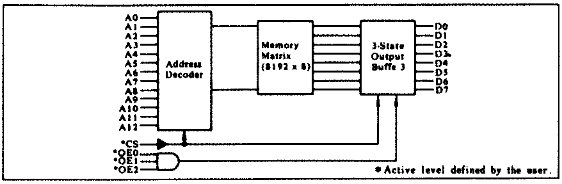


(FP-54)

■ FEATURES

- Fully Static Operation
- Automatic Power Down
- Single +5V Power Supply
- Three-state Data Output for OR-ties
- Mask Programmable Chip Select and Output Enable
- TTL Compatible
- Maximum Access Time; 250ns
- Low Power Standby and Low Power Operation; Standby 5μW (typ), Operation 50mW (typ)
- Pin Compatible with EPROM

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Supply Voltage*	V_{CC}	−0.3 to +7.0	V
Input Voltage*	V_{in}	−0.3 to +7.0	V
Operating Temperature	T_{opr}	−20 to +75	°C
Storage Temperature	T_{stg}	−55 to +125	°C
Bias Storage Temperature	T_{bias}	−20 to +85	°C

* with respect to V_{SS}

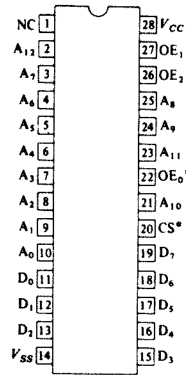
■ RECOMMENDED DC OPERATING CONDITIONS

Item	Symbol	min	typ	max	Unit
Supply Voltage *	V_{CC}	4.5	5.0	5.5	V
Input Voltage *	V_{IL}	−0.3	–	0.8	V
	V_{IH}	2.2	–	V_{CC}	V
Operating Temperature	T_{opr}	−20	–	75	°C

* with respect to V_{SS}

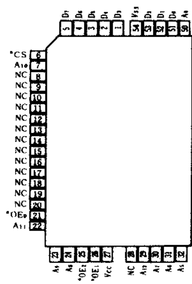
■ PIN ARRANGEMENT

- **HN61364P**



(Top View)

- **HN61364FP**



(Top View)

■ ELECTRICAL CHARACTERISTICS (V_{CC} = 5V±10%, V_{SS} = 0V, T_a = −20 to +75°C

Item		Symbol	Test Condition	min	typ**	max	Unit
Input High-level Voltage		V_{IH}		2.2	–	V_{CC}	V
Input Low-level Voltage		V_{IL}		−0.3	–	0.8	V
Output High-level Voltage		V_{OH}	I_{OH}=−205μA	2.4	–	–	V
Output Low-level Voltage		V_{OL}	I_{OL}=3.2mA	–	–	0.4	V
Input Leakage Current		I_{in}	V_{in}=0 to 5.5V	–	–	2.5	μA
Output High-level Leakage Current		I_{LOH}	V_{out}=2.4V, CS=0.8V, $\overline{CS}$=2.2V	–	–	10	μA
Output Low-level Leakage Current		I_{LOL}	V_{out}=0.4V, CS=0.8V, $\overline{CS}$=2.2V	–	–	10	μA
Supply Current	Active	I_{CC} *	V_{CC}=5.5V, I_{out}=0mA, t_{RC}=min, duty=100%	–	10	25	mA
	Standby	I_{SB}	V_{CC}=5.5V, $\overline{CS}\geq V_{CC}$−0.2V, CS≦0.2V	–	1	30	μA
Input Capacitance		C_{in}	V_{in}=0V, f=1MHz, T_a=25°C	–	–	10	pF
Output Capacitance		C_{out}		–	–	15	pF

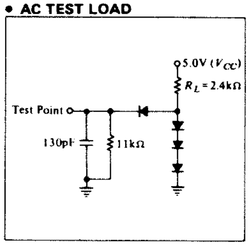
* Steady state current ** V_{CC} = 5V, T_a = 25°C

■ RECOMMENDED AC OPERATING CONDITIONS (READ SEQUENCE)

(V_{CC}=5V±10%, V_{SS}=0V, Ta=−20 to +75°C, t_r=t_f=20ns)

Item	Symbol	min	max	Unit
Read Cycle Time	t_{RC}	250	–	ns
Address Access Time	t_{AA}	–	250	ns
Chip Select Access Time	t_{ACS}	–	250	ns
Chip Selection to Output in Low Z	t_{CLZ}	10	–	ns
Output Enable to Output Valid	t_{OE}	–	100	ns
Output Enable to Output in Low Z	t_{OLZ}	10	–	ns
Chip Deselection to Output in High Z	t_{CHZ}	0	100	ns
Chip Disable to Output in High Z	t_{OHZ}	0	100	ns
Output Hold from Address Change	t_{OH}	10	–	ns

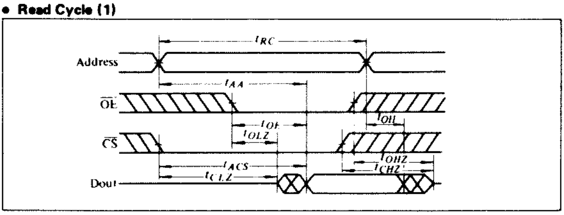
● **AC TEST LOAD**



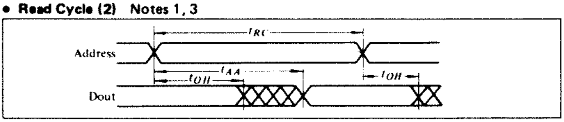
Notes) 1. t_r = t_f = 20ns
2. C_L includes jig capacitance.
3. All diodes are 1S2074Ⓗ.

■ TIMING WAVEFORM

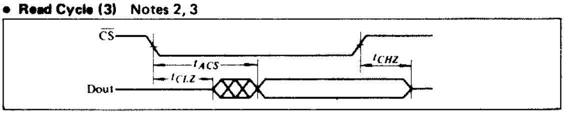
● **Read Cycle (1)**



● **Read Cycle (2)** Notes 1, 3



● **Read Cycle (3)** Notes 2, 3



NOTES:
1. Device is continuously selected.
2. Address Vaild prior to or coincident with $\overline{CS}$ transition low.
3. $\overline{OE}$ = V_{IL}
4. Input pulse level: 0.8 to 2.4V
5. Input and output reference level: 1.5V

Ⓜ MOTOROLA

MC14412

CMOS LSI

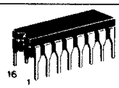
(LOW-POWER COMPLEMENTARY MOS)

UNIVERSAL LOW SPEED (0-600 bps) MODEM

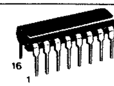
UNIVERSAL LOW SPEED MODEM (0-600 bps)

The MC14412 contains a complete FSK (Frequency-Shift Keying) modulator and demodulator compatible with both foreign (C.C.I.T.T. standards) and U.S.A. low speed (0 to 600 (bps) communication networks.

- On-Chip Crystal Oscillator with External Crystal
- Echo Suppressor Disable Tone Generator
- Originate and Answer Modes
- Simplex, Half-Duplex, and Full-Duplex Operation
- On-Chip Sine Wave Generator
- Modem Self Test Mode
- Single Supply:
  V_{DD} = 4.75 to 15 Vdc MC14412FP, MC14412 FL
  V_{DD} = 4.75 to 6.0 Vdc MC14412VP, MC14412VL
- Selectable Data Rates: 0-300, 0-600 bps
- Post Detection Filter
- TTL or CMOS Compatible Inputs and Outputs



L SUFFIX
CERAMIC PACKAGE
CASE 620

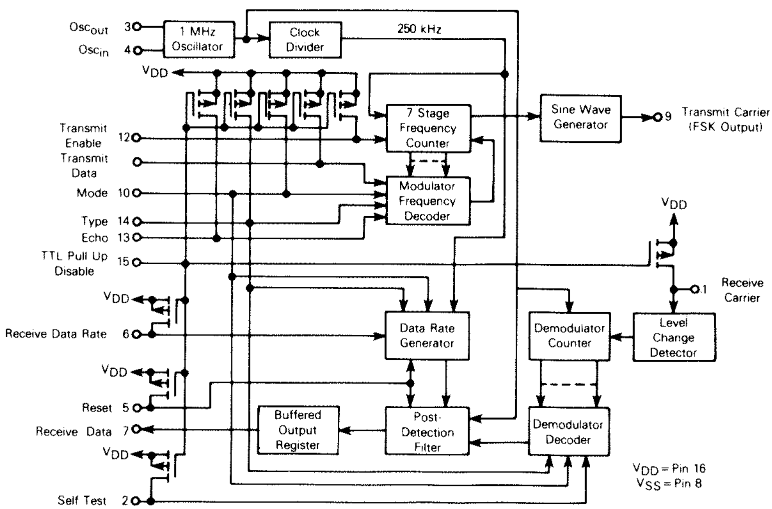


P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

MC144XX — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- F 4.75 to 15 Vdc
- V 4.75 to 6.0 Vdc

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD}** Vdc	−40°C Min	−40°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit
Output Voltage Pin 7 Only "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	V
$V_{in} = V_{DD}$ or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	V
$V_{in} = 0$ or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage* "0" Level										
(V_O = 4.5 or 0.5 V)	V_{IL}	5.0	–	1.5	–	2.25	1.5	–	1.5	V
(V_O = 9.0 or 1.0 V)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 V)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level Pin 15		5 to 15	V_{DD} − 0.75	–	V_{DD} − 0.8	V_{DD} − 2	–	V_{DD} − 0.85	–	
(V_O = 0.5 or 4.5 V)		5.0	3.5	–	3.5	2.75	–	3.5	–	
(V_O = 1.0 or 9.0 V)	V_{IH}	10	7.0	–	7.0	5.50	–	7.0	–	V
(V_O = 1.5 or 13.5 V)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current Pin 7 Only										
(V_{OH} = 2.5)	I_{OH}	5	−0.62	–	−0.5	−1.5	–	−0.35	–	mA
(V_{OH} = 9.5)		10	−0.62	–	−0.5	−1.0	–	−0.35	–	
(V_{OH} = 13.5)		15	−1.8	–	−1.5	−3.6	–	−1.1	–	
(V_{OL} = 0.4)	I_{OL}	4.75	2.3	–	2.0	4.0	–	1.6	–	mA
(V_{OL} = 0.5)		10	5.3	–	4.5	10	–	3.6	–	
(V_{OL} = 1.5)		15	15	–	13	35	–	10	–	
Input Current (Pin 15 = V_{DD})	I_{in}	–	–	–	–	±0.00001	±0.1	–	–	µA
Input Pull-Up Resistor Source Current (Pin 15 = V_{SS}, V_{in} = 2.4 Vdc) Pins 1, 2, 5, 6, 10, 11, 12, 13, 14	I_P	5	285	–	250	460	–	205	–	µA
Input Capacitance	C_{in}	–	–	–	–	5.0	–	–	–	pF
Total Supply Current (Pin 15 = V_{DD})	I_T	5	–	4.5	–	1.1	4.0	–	3.5	mA
		10	–	13	–	4.0	12	–	11	
		15	–	27	–	8.0	25	–	23	
Modulator/Demodulator Frequency Accuracy (Excluding Crystal)	ACC	5 to 15	–	–	–	0.5	–	–	–	%
Transmit Carrier Output 2nd Harmonic	V_{2H}	5	–	–	−20	−25	–	–	–	dB
		15	–	–	−25	−32	–	–	–	
Transmit Carrier Output Voltage (R_L = 100 kΩ) (Pin 9)	V_{out}	5	–	–	0.2	0.30	–	–	–	V_{RMS}
		10	–	–	0.5	0.85	–	–	–	
		15	–	–	1.0	1.5	–	–	–	
Maximum Receive Carrier Rise and Fall Times (Pin 1)	t_r, t_f	5	–	15	–	–	15	–	15	µs
		10	–	5.0	–	–	5.0	–	5.0	
		15	–	4.0	–	–	4.0	–	4.0	
Maximum Oscillator Frequency	f_{max}	5	–	–	1.2	5	–	–	–	MHz
Minimum Clock Pulse Width	t_w	5	–	–	–	50	350	–	–	ns

*DC Noise Immunity (V_{IL}, V_{IH}) is defined as the maximum voltage change from an ideal "0" or "1" input level, that the circuit will withstand before accepting an erroneous input.

**Note: Only 5-Volt specifications apply to MC14412VP devices.

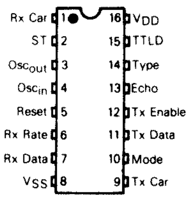
MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 8)

Rating	Symbol	Value	Unit
DC Supply Voltages MC14412FP, FL MC14412VP, VL	V_{DD}	−0.5 to 15 −0.5 to 6.0	V
Input Voltages, All Inputs	V_{in}	V_{DD} + 0.5 to V_{SS} − 0.5	V
DC Current Drain per Pin (except Pin 8, 7)	I	10	mA
DC Current Drain (Pin 8, 7)	I	35	mA
Operating Temperature Range	T_A	−40 to +85	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

PIN ASSIGNMENT



DEVICE OPERATION

GENERAL

Figure 1 shows the modem in a system application. The data to be transmitted is presented in serial format to the modulator for conversion to FSK signals for transmission over the telephone network. The modulator output is buffered/amplified before driving the 600 ohm telephone line.

The FSK signal from the remote modem is received via the telephone line and filtered to remove extraneous signals such as the local Transmit Carrier. This filtering can be either a bandpass which passes only the desired band of frequencies or a notch which rejects the known interfering signal. The desired signal is then limited to preserve the axis crossings and fed to the demodulator where the data is recovered from the received FSK carrier.

INPUT/OUTPUT FUNCTIONS

Figure 2 shows the I/O interface for the MC14412 low-speed modem. The following is a description of each individual signal.

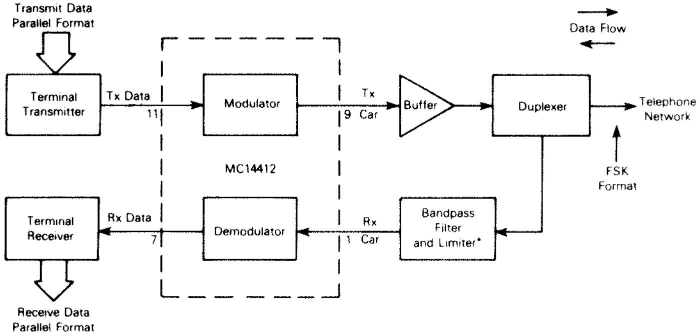
TYPE (Pin 14)

The Type input selects either the U.S. or C.C.I.T.T. operational frequencies for both transmitting and receiving data. When the Type input = "1", the U.S. standard is selected and when the Type input = "0", the C.C.I.T.T. standard is selected.

TRANSMIT DATA (Tx Data, Pin 11)

Transmit Data is the binary information input. Data entered for transmission is modulated using FSK techniques. When operating in the U.S. standard (Type = "1") a logic "1" input level represents a Mark or when operating in the CCITT standard (Type = "0") a logic "1" input level represents a Mark.

FIGURE 1 — TYPICAL LOW-SPEED MODEM APPLICATION



Since the modulator and demodulator sections of the MC14412 are functionally equivalent to those of the MC6860, additional application information can be obtained from the following Motorola publications:

AN-731 Low-speed Modem Fundamentals

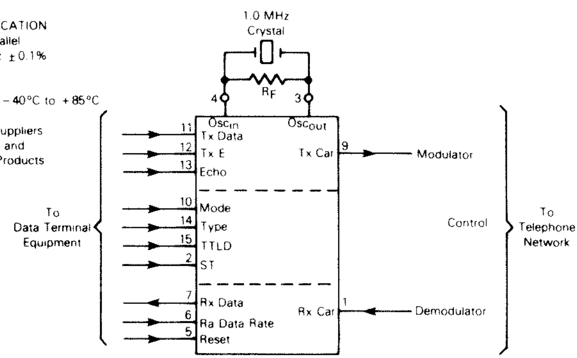
AN-747 Low-speed Modem System Design Using the MC6860

EB-49 Application Performance of the MC6860 MODEM.

FIGURE 2 — MC14412 INPUT/OUTPUT SIGNALS

*CRYSTAL SPECIFICATION
Crystal Mode — Parallel
Frequency — 1 MHz ±0.1%
$R_S = 540\ \Omega$ typ
$C_O = 7$ pF typ
Temperature Range −40°C to +85°C
Test Level — 1 mW
Suggested Crystal Suppliers
Tyco, CTS Knight and
Motorola Crystal Products

$R_F = 15$ mΩ ±20%



TRANSMIT CARRIER (Tx Car, Pin 9)

The Transmit Carrier is a digital-synthesized sine wave derived from a 1.0 MHz oscillator reference. The Tx CAR has an AC output impedance of 5 kΩ typical. The frequency characteristics are as follows:

United States Standard
Type = "1"
Echo = "0"

Mode		Tx Data		Tx Car
Originate	"1"	Mark	"1"	1270 Hz
Originate	"1"	Space	"0"	1070 Hz
Answer	"0"	Mark	"1"	2225 Hz
Answer	"0"	Space	"0"	2025 Hz

C.C.I.T.T. Standard
Type = "0"
Echo = "0"

Mode		Tx Data		Tx Car
Channel	"1"	Mark	"1"	980 Hz
No. 1	"1"	Space	"0"	1180 Hz
Channel	"0"	Mark	"1"	1650 Hz
No. 2	"0"	Space	"0"	1850 Hz

Echo Suppressor Disable Tone
Type = "0"
Echo = "1"

Mode	Tx Data	Tx Car
Chan. No. 2 "0"	"1"	2100 Hz

TRANSMIT ENABLE (Tx Enable, Pin 12)

The Transmit Carrier output is enabled when the Tx Enable input = "1". No output tone can be transmitted when Tx Enable = "0".

MODE (Pin 10)

The Mode input selects the pair of transmitting and receive frequencies used during modulation and demodulation. When Mode = "1", the U.S. originate mode is selected (Type input = "1") or the C.C.I.T.T. Channel No. 1 (Type input = "0"). When mode = "0", the U.S. answer mode is selected (Type input = "1") or the C.C.I.T.T. Channel No. 2 (Type input = "0").

ECHO (Pin 13)

When the Echo input = "1" (Type = "0", Mode = "0", Tx Data = "1") the modulator will transmit a 2100 Hz tone for disabling line echo suppressors. During normal data transmission, this input should be low = "0".

RECEIVE DATA (Rx Data, Pin 7)

The Receive Data output is the digital data resulting from demodulating the Receive Carrier.

RECEIVE CARRIER (Rx Car, Pin 1)

The Receive Carrier is the FSK input to the demodulator. This input must have either a CMOS or TTL compatible logic level input (see TTL pull-up disable) at a duty cycle of 50% ± 2%, that is a square wave resulting from a signal limiter.

RECEIVE DATA RATE (Rx Rate, Pin 6)

The demodulator has been optimized for signal to noise performance at 300, and 600 bps.

Data Rate	Rx Rate
0-300 bps	"1"
0-600 bps	"0"

SELF TEST (ST, Pin 2)

When a high level (ST = "1") is placed on this input, the demodulator is switched to the modulator frequency and demodulates the transmitted FSK signal.

RESET (Pin 5)

This input is provided to decrease the test time of the chip. In normal operation, this input may be used to disable the demodulator (Reset = "1") – otherwise it should be tied low = "0". The reset pin does not reset Rx data pin 7.

CRYSTAL (Osc_{in}, Osc_{out}, Pin 4, Pin 3, respectively)

A 1.0 MHz crystal is required to utilize the on chip oscillator. A 1.0 MHz square wave clock can also be applied to the Osc_{in} input to satisfy the clock requirement (see Figure 2).

When utilizing the 1.0 MHz crystal, external parasitic capacitance, including crystal shunt capacitance, must be < 9 pF at the crystal input (pin 4). Pin 4 is capable of driving only one CMOS input.

TTL PULL-UP DISABLE (TTLD, Pin 15)

To improve TTL interface compatibility, all of the inputs to the MODEM have controllable P-Channel devices which act as pull-up resistors when TTLD input is low ("0"). When the input is taken high ("1") the pull-up is disabled, thus reducing power dissipation when interfacing with CMOS. Pin 15 should be taken high ("1") with V_{DD} greater than 6 volts.

FIGURE 3 — M6800 MICROCOMPUTER FAMILY BLOCK DIAGRAM

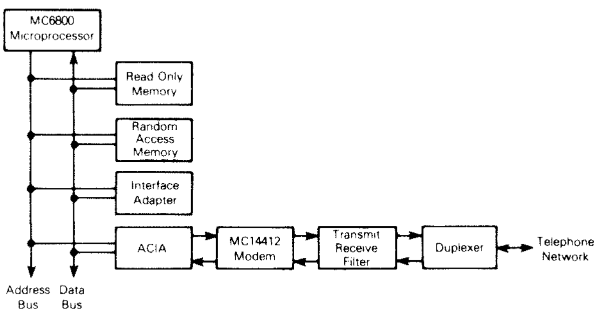


FIGURE 4 — TRANSMIT CARRIER SINEWAVE

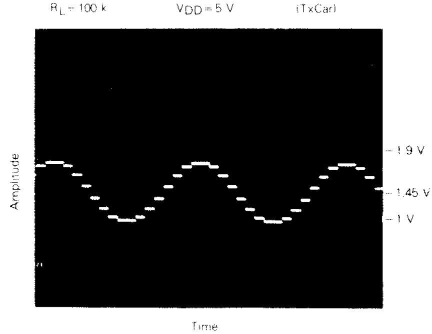
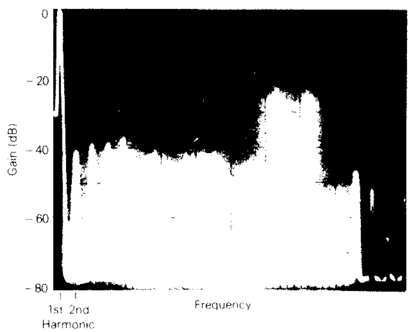
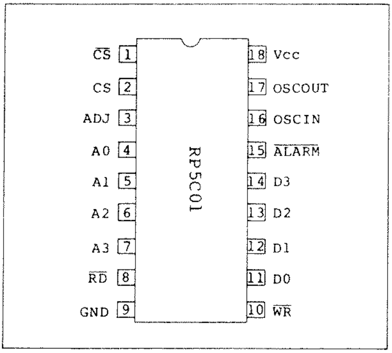


FIGURE 5 — TYPICAL TRANSMIT CARRIER FREQUENCY SPECTRUM



Outline:

The RP5C01 is a real-time clock that can be connected directly to the bus of microprocessors using the 8085A, Z80, 6809, 6502 or other CPU. Time can then be written to or read from the clock in the same way as writing to or reading from RAM. As well as calendar and time counters and alarm function, the RP5C01 has a 26 x 4-bit RAM, allowing battery backup. It can therefore be used as a non-volatile RAM.

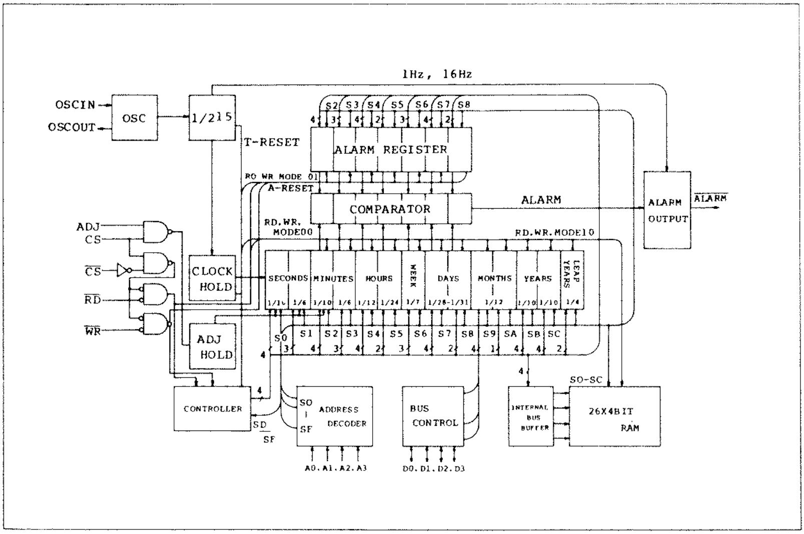


Features:

* Direct connection to CPU
* 4-bit bidirectional bus D0-D3
* 4-bit address inputs A0-A3
* Internal counters for time (hours, min., sec.) and date (100 years, leap years, months, days, and days-of-the-week)
* Choice of 24-hour or 12-hour (AM/PM) system
* All clock data expressed in BCD code
* ±30 sec. adjustment function
* Provision for battery backup
* Internal 26 x 4-bit RAM
* Alarm signal, 16 Hz clock signal or 1 Hz clock signal output

Terminal connection diagram

Block diagram



Absolute max. ratings

Symbol	Item	Conditions	Values	Units
V_{CC}	Supply voltage		-0.3 - 7	V
V_I	Input voltage	Voltage at any pin with respect to GND	-0.3 - 7	V
V_O	Output voltage		-0.3 - 7	V
Pd	Max. power consumption	Ta=25°C	700	mW
Topg	Under bias		0 - 70	°C
Tstg	Storage temperature		-40 - 125	°C

Recommended operating conditions (Ta=0 - 70°C unless otherwise specified)

Symbol	Item	Values			Units
		Min	TYP	Max.	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{DH}	Data preservation voltage	2.2		5.5	V
f_{XT}	Oscillation frequency of crystal oscillator		32.768		kHz

DC electrical characteristics

Ta=0 - 70°C, Vcc=5V ±10% unless otherwise specified.

Symbol	Item	Measurement conditions	Values			
			Min.	TYP	Max.	Units
V_{IH}	"H" input voltage		2.0		Vcc	V
V_{IL}	"L" input voltage		-0.3		0.8	V
V_{OH}	"H" output voltage	I_{OH}=-400μA	2.4			V
V_{OL}	"L" output voltage	I_{OL}=2mA			0.4	V
I_I	Input current	V_I=0 - 5.5V			±10	μA
I_{OZ}	Output leakage current				±10	μA
I_{CC1}	Vcc power supply current	f_{XT}=32.768kHz Vcc=2.2V			15	μA
I_{CC2}	Vcc power supply current	f_{XT}=32.786kHz Vcc=5.0V (Note 2)			250	μA

Note 1: current towards IC is considered positive (no sign)

Note 2: When connected to CPU (read/write cycle 10μs)

AC electrical characteristics

(Ta=0 - 70°C, Vcc=5V ±5% unless otherwise specified)

Symbol		Measurement conditions	Values Min.	TYP	Max.	Units
t_{AC}	Address $\overline{RD}/\overline{WR}$ delay time		170			ns
t_{CC}	$\overline{RD}/\overline{WR}$ pulse width		400		10000	ns
t_{CA}	Address valid time after $\overline{RD}/\overline{WR}$ leading edge		10			ns
t_{RD}	Data delay time after $\overline{RD}$ trailing edge				400	ns
t_{RDH}	Data hold time after $\overline{RD}$ leading edge		0			ns
t_{WDL}	Data delay time after $\overline{WR}$ trailing edge				40	ns
t_{WD}	Data hold time after $\overline{WR}$ leading edge		20			ns

AC electrical characteristics are as follows when Vcc=5V ±10%.

Symbol		Measurement conditions	Values Min.	TYP	Max.	Units
t_{AC}	Address $\overline{RD}/\overline{WR}$ delay time		170			ns
t_{CC}	$\overline{RD}/\overline{WR}$ pulse width		450		10000	ns
t_{CA}	Address valid time after $\overline{RD}/\overline{WR}$ leading edge		10			ns
t_{RD}	Data delay time after $\overline{RD}$ trailing edge				400	ns
t_{RDH}	Data hold time after $\overline{RD}$ leading edge		0			ns
t_{WDL}	Data delay time after $\overline{WR}$ trailing edge				40	ns
t_{WD}	Data hold time after $\overline{WR}$ leading edge		20			ns

*Refer to the timing chart of page 51 to check the symbols.

Function of pins

Name of pin	No. of pin	Function
$\overline{CS}$, CS	1,2	External interface terminals, valid when CS = H and $\overline{CS}$ = L. CS is connected to the power-down detector of the peripheral circuitry and $\overline{CS}$ to a CPU address decoder.
ADJ	3	For easy adjustment of the second counter without connection to a CPU. If ADJ is set to high when the second counter registers 0 - 29, the seconds are set to 0, and if ADJ is set to high when the second counter registers 30 - 59, the seconds are set to 0 and the minutes are incremented. This terminal is designed not for edge detection but for level detection. A minimum of 100 μsec. is required for high-level adjustments.
A_0 - A_3	4,5,6,7	Address terminals. Connected to address bus of CPU.
$\overline{RD}$	8	I/O control terminal. Low when RP5C01 is read by CPU.
GND	9	0V
$\overline{WR}$	10	I/O control terminal. Low when RP5C01 is written by CPU.
D_0 - D_3	11,12,13,14	Bidirectional data bus. Connected to data bus of CPU.
$\overline{ALARM}$	15	For output of alarm signal or 16Hz/1Hz clock signals. Open-drain output.
OSCIN, OSCOUT	16 17	For connection to 32.768kHz crystal oscillator circuit.
Vcc	18	+5V power supply terminal

Address allocation of MODE 00 (Note 1)

MODE	MODE 00				
A3 - A1	Contents	D3	D2	D1	D0
0	1-sec counter				
1	10-sec counter	x			
2	1-min counter				
3	10-min counter	x			
4	1-hour counter				
5	10-hour counter (Note 2)	x	x		
6	Day-of-the-week counter	x			
7	1-day counter				
8	10-day counter	x	x		
9	1-month counter				
A	10-month counter	x	x	x	
B	1-year counter				
C	10-year counter				
D	MODE Register	Timer EN	Alarm EN	MODE selector	
				M1	M0
E	Test Register	Test 3	Test 2	Test 1	Test 0
F	RESET Controller	$\overline{1Hz\ ON}$	$\overline{16Hz\ ON}$	Timer RESET	Alarm RESET

X indicates that the counter may take any value during write operations, but always be 0 when read out.

(Note 1) MODE 00 is set by writing data (X,X,0,0) to address D.
(Note 2) Bit 1 of the 10-hour counter should be as follows when the 12-hour system is selected:
D1 = 1 (PM)
D1 = 0 (AM)

Address allocation of MODE 01 (Note 1)

MODE		MODE 01			
A3–A1	Contents	D3	D2	D1	D0
0		x	x	x	x
1		x	x	x	x
2	Alarm 1-min register				
3	Alarm 10-min register	x			
4	Alarm 1-hour register				
5	Alarm 10-hour register	x	x		
6	Alarm day-of-the-week register	x			
7	Alarm 1-day register				
8	Alarm 10-day register	x	x		
9		x	x	x	x
A	12-$\overline{\text{hour}}$/24-hour selector	x	x	x	
B	Leap-year counter	x	x		
C		x	x	x	x
D	Mode Register	Timer EN	Alarm EN	MODE selector M1	M0
E	Test Register	Test 3	Test 2	Test 1	Test 0
F	Reset Controller	$\overline{\text{1Hz}}$ $\overline{\text{ON}}$	$\overline{\text{16Hz}}$ $\overline{\text{ON}}$	Timer RESET	Alarm RESET

(Note 1) MODE 01 is set by writing data (X,X,0,1) to address D.

Address allocation of MODE 10 and 11 (Note 1)

MODE	MODE 10 (RAM)				MODE 11 (RAM)			
A_3~A_1	Contents				Contents			
0								
1								
2	block 10				block 11			
3								
4								
5	4 bit				4 bit			
6	x				x			
7	13				13			
8								
9	RAM				RAM			
A								
B								
C								
D	Timer EN	Alarm EN	MODE selector M1	M0	Timer EN	Alarm EN	MODE selector M1	M0
E	Test 3	Test 2	Test 1	Test 0	Test 3	Test 2	Test 1	Test 0
F	1Hz $\overline{\text{ON}}$	$\overline{\text{16Hz}}$ $\overline{\text{ON}}$	Timer RESET	Alarm RESET	$\overline{\text{1Hz}}$ $\overline{\text{ON}}$	$\overline{\text{16Hz}}$ $\overline{\text{ON}}$	Timer RESET	Alarm RESET

(Note 1) MODE 10 is set to by writing data (X,X,1,0) to address D.
MODE 11 is set by writing data (X,X,1,1) to address D. (MODE 10 and 11 are in RAM areas)

* Mode register (A3,A2,A1,A0) = (1,1,0,1) = D

```
  D3     D2     D1     D0
 Timer  Alarm
  EN     EN     M1     M0
  |      |
  |      |      0      0    MODE 00: setting or reading time
  |      |      0      1    MODE 01: setting or reading of Alarm
  |      |                           data, 12/24 hour system, or
  |      |                           leap year
  |      |      1      0    Writing to or reading Block 10 in RAM
  |      |      1      1    Writing to or reading Block 11 in RAM
  |      |
  |      └------------------> Set 1 to enable alarm output.
  |                           Set 0 to disable alarm output (16Hz/
  |                           1Hz clock signals not affected)
  |
  └-------------------------> Set 1 to start clock.  Set 0 to stop
                              seconds and subsequent counters.
```

* The leap-year counter registers a leap year when D1 = D0 = 0. It simultaneously counts with the year counter.
* The $\overline{\text{12-hour}}$/24-hour selector sets the 12-hour system when D0 = 0 and the 24-hour system when D0=1. PM or AM is selected when D1 in the 10-hour counter is 1 or 0, respectively (see page 47).
* Reset controller 16Hz/1Hz clock register.

  (A3,A2,A1,A0) = (1,1,1,1) = F

  D0 = 1: resets all alarm registers and internal Alarm F/Fs.

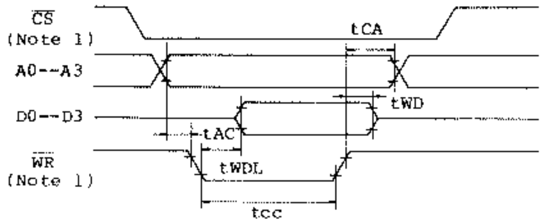
  D1 = 1: resets the 15-stage dividers before the seconds register.

  D2 = 0: switches on the 16Hz clock pulse generated from the $\overline{\text{ALARM}}$ terminal.

  D3 = 0: switches on the 1Hz clock pulse generated from the $\overline{\text{ALARM}}$ terminal.
* Addresses 0--D: able to read and write.
* Addresses E--F: only able to write and 0H always appears when read out.

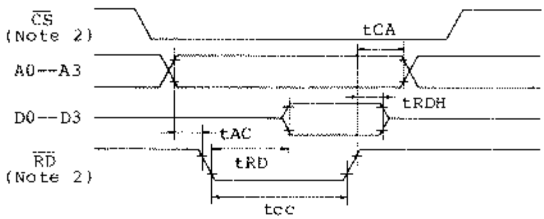
Timing chart

WRITE CYCLE (CS = "H")



(Note 1) The RP5C01 accepts a $\overline{WR}$ signal when both $\overline{CS}$ = low and CS = high. The timing of $\overline{CS}$ is not specified, but because of the construction of the RP5C01, the $\overline{WR}$ signal in the above diagram should be taken as the CS·$\overline{CS}$·$\overline{WR}$ signal. (For details, see the block diagram of the RP5C01 or Section 4 of these Application Notes.)

READ CYCLE (CS = "H")



(Note 2) The RP5C01 accepts an $\overline{RD}$ signal when both $\overline{CS}$ = low and CS = high, in the same way as for a $\overline{WR}$ signal. The $\overline{RD}$ signal in the above diagram should therefore be taken as the CS·$\overline{CS}$·$\overline{RD}$ signal in the same way as the $\overline{WR}$ signal. (For details, see the block diagram of the RP5C01 or Section 4 of these Application Notes.)

Application Notes

(1) Oscillator circuit

(1-1) When constructing the oscillator circuit using a crystal oscillator.

The oscillator circuit should be constructed as shown in Fig. 1. External components needed are a resistor, a condenser, and a trimmer condenser for fine adjustment of the frequency. The oscillation frequency should be adjusted by altering the value of the trimmer condenser using the standard 16Hz or 1Hz clock signal output from the $\overline{\text{ALARM}}$ terminal.

When adjusting with the 16Hz signal:

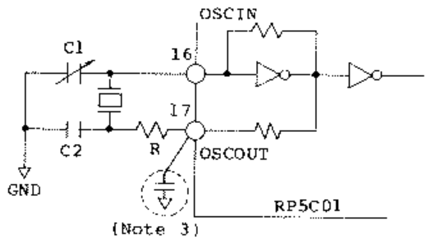
Address: (A3,A2,A1,A0) = (1,1,1,1)

Data: (1,0,0,0)

When adjusting with the 1Hz signal:

Address: (A3,A2,A1,A0) = (1,1,1,1)

Data: (0,1,0,0)



C1 = 10PF--30PFr
C2 = 30PFr (Note 3)
R = 100kΩ
Crystal oscillator: Nihon Denpa Kogyo MX38T

Fig. 1

(Note 3) Different values of C1, C2, and R may be used, and the crystal oscillator is not definitely specified. The values of C1, C2, and R noted above are the best values for the MX38T oscillator used in the measurements carried out by Ricoh.
A bypass condenser set between pin 17 and GND is sometimes effective for external noise. Its value should be less than 60 PFr according to the measurements. For details, see Section 1 of these Application Notes.

(1-2) When using an external clock

When an external clock is used, the arrangement shown in Figs. 2-(a) and 2-(b) below should be adopted. The OSCIN terminal is not TTL-compatible but CMOS-compatible.

1) With CMOS inverter

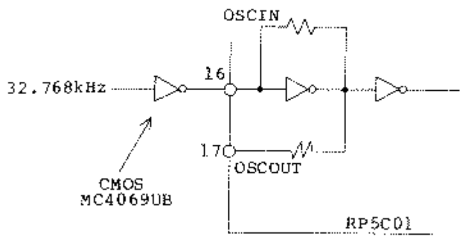


Fig. 2-(a)

2) With TTL inverter

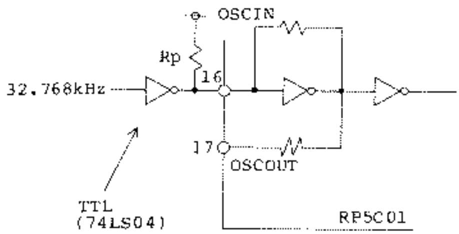


Fig. 2-(b)

(2) Input/output terminals and chip selection terminals

(2-1)Input/output terminals

Pull-up (4.7-47kΩ) or pull-down (100-300kΩ) resistors should be installed to fix the potentials of the I/O terminals during battery backup. (See Note 4 on page 55.)

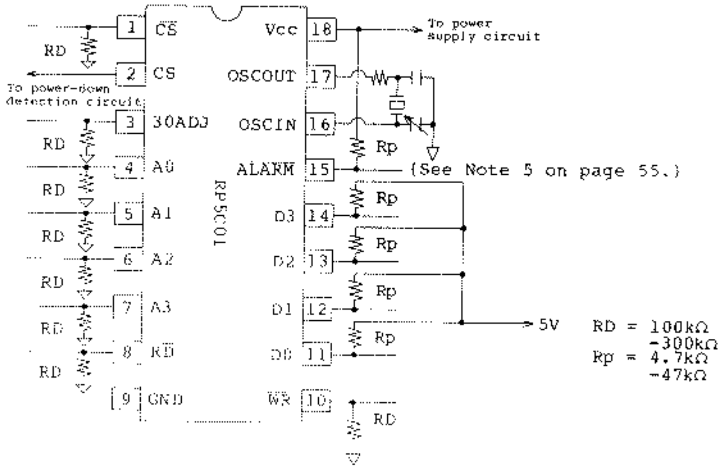


Fig. 3

(2-2) Chip select terminals

Two chip select terminals are provided. The CS terminal should be connected to the power-down detection circuit and the $\overline{\text{CS}}$ terminal to the CPU. CS is active when high and $\overline{\text{CS}}$ is active when low.

(Note 4)

The values of the pull-up and pull-down resistors need not necessarily be those given above (4.7--47kΩ and 100--300kΩ, respectively), but they should be chosen so that the RP5C01's DC characteristics VIH, VIL, VOH and VOL are satisfied. These resistors are used to maintain the level of the I/O terminals (D0--D3) and the input terminals at any time (e.g., during battery backup), and they have the effect of reducing the current consumption during battery backup. It is immaterial whether pull-up or pull-down resistors are selected for any of the I/O or input terminals. However, it is recommended that pull-up resistors be used for $\overline{CS}$, $\overline{RD}$, and $\overline{WR}$, since if pull-down resistors are used for these terminals, they will become active when the CPU is on hold (e.g.,at DMA cycle, control lines of $\overline{CS}$, $\overline{RD}$, and $\overline{WR}$ start to float instantaneously) and this may lead to problems. The arrangement of resistors shown in Fig. 3 is an example only, and may be altered. For details, see Section 3 of these Application Notes.

(Note 5)

If terminal 15 (the $\overline{ALARM}$ terminal) is to be used during battery backup, it should be pulled up by the same battery power source as the RP5C01. If it is not to be used during battery backup, it should be pulled up by the system power source, which cannot supply voltage during power down.

TANDY 200 ROM INFORMATION

USA/CANADA VERSION

These pages provide essential information for using ROM functions.

LCD Functions

Function Name	Description	Entry Address (Hex.)
LCDPUT	Displays a character on the LCD at current cursor position. (Also RST 4) Entry condition: A = character to be displayed Exit condition: none	503C
SETCUR	Move cursor to specified location. Entry conditions: D = x coordinate (1-40) E = y coordinate (1-16) Exit condition: none	8D6A
PLOT	Turn on pixel at specified location. Entry conditions: D = x coordinate (0-239) E = y coordinate (0-127) Exit condition: none	8D76
UNPLOT	Turn off pixel at specified location. Entry conditions: D = x coordinate (0-239) E = y coordinate (0-127) Exit condition: none	8D77
POSIT	Set cursor position. Entry conditions: H = column number (1-40) L = row number (1-16) Exit condition: none	4F9B
ESCA	Send specified Escape Code Sequence. Entry conditions: A = escape code Exit condition: none	4F8F

Routines for Generating Common LCD Functions and Escape Codes

Function Name	Description	Entry Address (Hex.)	Equiv. ESC
CRLF	Generate a Carriage Return and Line Feed on LCD	4F3E	—
HOME	Move cursor to Home position (1,1)	4F49	—
CLS	Clear display	4F4D	—
SETSYS	Set system line (lock line 16, LABEL)	4F54	T
RSTSYS	RESET system line (unlock line 16, LABEL)	4F59	U
LOCK	Lock display (no scrolling)	4F5E	V
UNLOCK	Unlock display (scrolling)	4F63	W
CURSON	Turn on cursor	4F68	P
CURSOF	Turn off cursor	4F6D	Q
DELLIN	Delete line at current cursor position	4F72	M
INSLIN	Insert a blank line at cursor position	4F77	L
ERAEOL	Erase from cursor to end of line	4F7C	K
ENTREV	Set Reverse character mode	4F88	p
EXTREV	Turn off Reverse character mode	4F8D	q

Variable and Status Locations

Name Contents	Address
CSRY Cursor Position (ROW)	EF06
CSRX Cursor Position (Column)	EF07
BEGLCD Start of LCD memory	FA30
ENDLCD End of LCD memory	FCAF

Keyboard Functions

Function Name	Description	(Hex.) Entry Address
KYREAD	Scan keyboard for a key, return with or without one. Entry conditions: none Exit conditions: A = Character, if any Z flag — set if no key found — reset if key found Carry — set (character in code table below) — reset (normal character set code) **Resister A** / **Key pressed** 0 F1 1 F2 2 F3 3 F4 4 F5 5 F6 6 F7 7 F8 8 LABEL 9 PRINT 0A SHIFT-PRINT 0B PASTE	8B03
CHGET	Wait and get character from keyboard. Entry conditions: none Exit conditions: A = character code Carry — set if special character — reset if normal character (F1 - F8 return preprogrammed strings)	12F7
CHSNS	Check keyboard queue for characters Entry conditions: none Exit conditions: Z flag set if queue empty, reset if keys pending	1404
KEYX	Check keyboard queue for character or BREAK. Entry conditions: none Exit conditions: Z flag set if queue empty, reset if keys pending Carry — Set when BREAK entered — Reset with any other key	8B31

Keyboard Functions

Function Name	Description	(Hex.) Entry Address
BRKCHK	Check for BREAK characters only (CTRL-C or -S) Entry conditions: none Exit conditions: Carry — set if BREAK or PAUSE entered — reset if no BREAK characters	8B4D
INLIN	Get line from keyboard (terminated by ENTER) Entry conditions: none Exit conditions: data stored at location F685	54F6

Using Function Keys Routines

The function table consists of character strings to be used by the keyboard driver when processing F1 - F8 keys. The strings have maximum length of 16 characters and are terminated by a "80" (Hex.) code. If the last character of the string is OR'ed with 80, the character will also serve as a terminator. The entire string will be placed in the keyboard buffer when the appropriate strings for all 8 keys are pressed. You must specify character strings for all 8 function keys (use the terminator bytes for any you wish to ignore).

Example of function table:

```
FCTAB    DEFM    'Files'     ;  F1
         DEFW    0D80
         DEFM    'Load'      ;  F2
         DEFB    80
         DEFM    'Save'      ;  F3
         DEFB    80
         DEFM    'Run'       ;  F4
         DEFW    0D80
         DEFM    'List'      ;  F5
         DEFW    0D80
         DEFB    80          ;  Ignore F6
         DEFB    80          ;  Ignore F7
         DEFM    'Menu'      ;  F8
         DEFW    OD80
```

Function Name	Description	(Hex.) Entry Address
STFNK	Set function key definitions Entry conditions: HL = Address of function table (above) Exit conditions: none	6E20
CLFNK	Clear function key definition table (fills with 80's) Entry conditions: none Exit conditions: none	6E1D
DSPFNK	Display function keys Entry conditions: none Exit conditions: none	4FC7
STDSPF	Set and display function keys Entry conditions: HL = Start address of function table Exit conditions: none	4FC4
ERAFNK	Erase function key display Entry conditions: none Exit conditions: none	4FA9
FNKSB	Display function table (if enabled) Entry conditions: none Exit conditions: none	6E42

Printing Routines

Function Name	Description	(Hex.) Entry Address
PRINTER	Send a character to the line printer Entry conditions: A = character to be printed Exit conditions: Carry — set if cancelled by BREAK — reset if normal return	84C9
CHPLPT	Print character without expanding tab characters Entry conditions: A = character to be printed Exit condition:	1590
OUTDLP	Print a character expanding tabs to spaces Entry conditions: A = character to be printed Exit conditions:	5A14

Function Name	Description	(Hex.) Entry Address
LCOPY	Print contents of LCD Entry conditions: none Exit conditions: none	2946

RS232-C and MODEM Routines

Function Name	Description	(Hex.) Entry Address
DISHHC	Disconnect Phone Line Entry conditions: none Exit conditions: none	61BA
CONHHC	Connect phone line Entry conditions: none Exit conditions: none	61D0
ATDIAL	Dial a specified phone number Entry conditions: HL=ph. number address Exit conditions: none	622B
RCVX	Check RS232C queue for characters Entry conditions: none Exit conditions: A=number of characters in queue Z flag — set if no data — reset if characters pending	8508
RV232C	Get a character from RS232 receive queue Entry conditions: none Exit conditions: A=character received Z flag — set if O.K. — reset if error (PE,FF, or OF) Carry — set if BREAK pressed, else reset	8519
SNDCQ	Send an XON resume character (CTL-Q) Entry conditions: none Exit conditions: none	8608
SNDCS	Send an XOFF pause character (CTL-S) Entry conditions: none Exit conditions: none	8617

Function Name	Description	(Hex.) Entry Address
SD232C	Send a character to the RS232 or Modem (with XON/XOFF) Entry conditions: A = character to be sent Exit conditions: Carry — set if BREAK pressed, else reset	8643
CARDET	Detect carrier Entry conditions: none Exit conditions: A = 0 if carrier Z flag — set if carrier, else reset	874A
SNDCOM	Send a character to RS232-C or modem (without XON/XOFF flow control) Entry conditions: C = character to be sent Exit conditions: Carry — set if BREAK pressed, else reset	8629
BAUDST	Set Baud rate for RS232-C Entry conditions: H = Baud rate (1-9, M) Exit conditions: none	86AD
INZCOM	Initialize RS232-C and Modem Entry conditions: H = Baud rate (1-9) L = USART configuration code USART = 8251 Carry — set if RS232-C — reset if modem Exit conditions: none	86DE

BIT(S)	Description
0-1	Baud rate: 00 = None, 10 = X1 01 = X16(fix), 11 = X64
2-3	Word length: 00 = 5, 10 = 6, 01 = 7, 11 = 8
4	Parity enable: 0 = Disable 1 = Enable
5	Parity setting: 0 = ODD 1 = Even
6-7	Specifies number of Stop Bits: 00 = None 10 = 1, 01 = 1.5, 11 = 2

The text string containing the current STAT setting is located at EF3CH (7 bytes): Baud, Length, Parity, Stop bits, XON/XOFF switch, Ignore control and Ignore LF.

Function Name	Description	(Hex.) Entry Address
SETSER	Set serial interface parameters and activate RS232-C/Modem Entry conditions: HL = start address of ASCII string containing parameters terminated by a binary zero ('78E1ENN,0). Syntax same as in Telecom's STAT Carry — set for RS232-C — reset for Modem Exit conditions: none	191D
CLSCOM	Deactivate RS232-C/Modem Entry conditions: none Exit conditions: none	87B5

Cassette Recorder Routines

Function Name	Description	(Hex.) Entry Address
DATAR	Read character from cassette (no checksum) Entry Conditions: none Exit conditions: D = character from cassette Carry — Set if BREAK pressed, else reset	88B3
CTON	Turn motor on Entry conditions: none Exit conditions: none	15C0
CTOFF	Turn motor off Entry conditions: none Exit conditions: none	15C2
CASIN	Read a character from cassette and update checksum Entry conditions: C = current checksum Exit conditions: A = character C = contains the updated checksum	15C8
	Send characters to cassette and update checksum Entry conditions: A = character to be sent C = current checksum Exit conditions: C = updated checksum	15D9

Function Name	Description	(Hex.) Entry Address
SYNCW	Write cassette header and sync byte only Entry conditions: none Exit conditions: Carry — Set if BREAK pressed, else reset	87D1
SYNCR	Read cassette header and sync byte only Entry conditions: none Exit conditions: Carry — set if BREAK pressed, else reset	8810
DATAW	Write a character to cassette (no checksum) Entry conditions: A = character to be sent Exit conditions: Carry — set if BREAK pressed, else reset	87E6

RAM Files Routines

The Directory Table (located at F252) contains all file location, type, and status information.

Each file is managed by an 11-bytes directory entry in the format:

Byte 1	:	Directory Flag (for file type and status)
Byte 2-3	:	Address of file
Byte 4-11	:	8 Byte filename

The Directory Flag contains the following information:

Bit 7 (MSB)	1 if a valid entry
Bit 6	1 for ASCII text file (DO)
Bit 5	1 for Machine language (CO)
Bit 4	1 for ROM file
Bit 3	1 for invisible file
Bit 2	reserved for future use
Bit 1	reserved for future use
Bit 0	internal use only

Function Name	Description	(Hex.) Entry Address
MAKTXT	Create a text file Entry conditions: filename (max. 8 bytes) must be stored in FILNAM(F746).'DO' extension not required Exit conditions: HL = TOP address of new file DE = address of Directory entry (Flag) Carry — set if file already exists — reset if new file	2D7C
CHKDC	Search for file in directory Entry conditions: DE = address of filename to find (ASCII filename + 0 byte terminator) Exit conditions: HL = start address (TOP) of file Z Flag — 0 (file found) 1 (file not found)	6E4D
GTXTTB	Get top address of file Entry conditions: HL = address of directory entry for file Exit conditions: HL = TOP start address of file	6E8C
KILASC	Kill a text (DO) file Entry conditions: DE = file TOP start address HL = address of directory entry (flag) Exit conditions: none	2AB5
INSCHR	Insert a character in a file Entry conditions: A = character to insert HL = address to insert character Exit conditions: HL = +1 Carry — set if out of memory	829C
MAKHOL	Insert a specified number of spaces in a file Entry conditions: BC = number of spaces to insert HL = address to insert spaces Exit conditions: HL & BC are preserved Carry — set if out of memory	82A8
MASDEL	Delete specified number of characters Entry conditions: BC = number of characters to delete HL = address of deletion Exit conditions: HL & BC are preserved	82DA

Other Routines

Function Name	Description	(Hex.) Entry Address
INITIO	Cold start reset Entry condition: none Exit condition: none	841C
IOINIT	Warm start Menu Entry condition: none Exit condition: none	8439
MENU	Go to Main Menu Entry conditions: none Exit conditions: none	67A4
MUSIC	Make tone (see owner's manual for frequency and duration information) Entry conditions: DE = frequency (0 - 16383) B = duration (0 - 255) Exit conditions: none	8BC0
TIME	Read system TIME Entry conditions: HL = address of 8 byte area for TIME Exit conditions: HL = TIME (hh:mm:ss)	1A7E
DATE	Read system DATE Entry conditions: HL = address of 8 byte area for DATE Exit conditions: HL = DATE (mm/dd/yy)	1A9E
DAY	Read system DAY of the week Entry conditions: HL = address of 3 byte area for DAY Exit conditions: HL = DAY (add)	1AC5

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